SIDDAGANGA INSTITUTE OF TECHNOLOGY,

TUMAKURU 572103, KARNATAKA, INDIA

DEPARTMENT OF ELECTRONICS AND INSTRUMENTATION ENGINEERING

SYLLABUS

FOR

PG Course in

VLSI Design and Embedded Systems

2026-27

Siddaganga Institute of Technology, Tumkur-572103
Department of Electronics & Instrumentation Engineering

Programme: M.Tech - VLSI Design and Embedded Systems

Vision of the Institute

To develop thoughtful and creative young minds in a learning environment of high academic ambience by synergizing spiritual values and technological competence.

Mission of the Institute

1. To continuously strive for the total development of students by educating them in state-of-the-art-technologies and managerial competencies providing best in class learning experience with emphasis on skills, values and learning outcomes and helping them imbibe professional ethics and societal commitment.
2. To create a research ambience that promotes interdisciplinary research catering to the needs of industry and society.
3. To collaborate with premier academic and research institutions and industries to strengthen multidisciplinary education, applied research, innovation, entrepreneurship and consulting ecosystems.

Quality Policy

Siddaganga Institute of Technology is Committed to:

1. Impart Quality Education by establishing effective learning - teaching - learning processes to
   produce competent engineers and managers with high professional ethics and societal
   responsibility.
2. Create congenial environment and provide state-of the-art infrastructure.
3. Continually improve the effectiveness of the Quality Management System.
4. Satisfy applicable requirements.

Vision of the Department

To become a premier Electronics and Instrumentation Engineering Department by imparting quality education in the fields of electronics, instrumentation and cutting edge technologies developing competence to meet industrial norms and to pursue research and innovation contributing to socioeconomic development.

Mission of the Department

1. Develop competent professionals by offering industry aligned curriculum in Electronics, Instrumentation and VLSI and embedded systems along with an exposure to cutting edge technologies by providing best in class learning, promoting interdisciplinary research and innovation catering to industrial and societal needs.
2. Encourage and prepare students for higher studies to promote lifelong learning.
3. Imbibe professional ethics and skills in students to provide engineering service to the society.
4. Collaborate with industries to inculcate industry readiness, creativity, managerial competence, experiential learning and entrepreneurship skills.

Program Educational Objectives (PEOs):

PEO1: To build their **career in the core industry, public sector or multinational corporations**, in the domain of VLSI Design and Embedded systems.

PEO2: To engage in lifelong learning, excel in **research pursuits** and entrepreneur in technologies related to VLSI and Embedded Systems to meet the global challenges.

PEO3: To consistently exhibit **professional** and **ethical values**, **communication skills**, **team work and leadership** quality in their profession for the benefit of the society.

Program Outcomes (POs):

PO1 (Team Work): An ability to independently carry out research/investigation and development work to solve practical problems.

PO2 (Communication): An ability to write and present a substantial technical report/document.

PO3 (Scholarship of Knowledge): Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PO4 (Problem Solving): The student will be able to think and solve engineering problems, evaluate a wide range of potential solutions for those problems, and arrive at feasible/optimal solutions.

PO5 (Usage of Modern Tools): The student will be able to apply modern engineering tools, equipment, and techniques to model and predict complex engineering problems with an understanding of the limitations.

PO6 (Project Management): The student will demonstrate knowledge and understanding of engineering and management principles and apply the same to one's own work, as a member and leader in a team, to manage projects efficiently and economically.

PO7 (Life-long Learning): The student will be able to recognize the need for, and demonstrate the ability to engage in lifelong learning independently with a high level of enthusiasm and commitment to improve knowledge and competency continuously.

Programme Specific Outcomes (PSOs):

PSO1: Apply the technical knowledge to **analyse, design, and implement VLSI system** and apply advanced concept in the field of semiconductor and emerging technologies.

PSO2: Apply the knowledge of **embedded system and Programming Skills** to design electronic system for real time applications.

SIDDAGANGA INSTITUTE OF TECHNOLOGY, TUMAKURU-03

(An autonomous Institute under Visvesvaraya Technological University)

SCHEME OF TEACHING AND EXAMINATION

I SEMESTER M.Tech. VLSI Design and Embedded Systems

I SEMESTER

Sl. No.	Course Type	Course Code	Course Title	Teaching & Learning Scheme					Examination				Credits
				CI		LI	TW & SL	Total Hours /Sem	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P							
1	PCC	P1LVS1	ARM Microcontroller and Applications	42	0	0	48	90	03	50	50	100	3
2	PCC	P1LVS2	Machine Learning for Electronics Engineers	42	0	0	48	90	03	50	50	100	3
3	PCC	P1LVS3	Analog ICs Design	42	0	0	48	90	03	50	50	100	3
4	IPCC	P1LVSI4	VLSI Design	42	0	28	50	120	03	50	50	100	4
5	PEC-I	P1LVSE1X	Professional Elective Course-I	42	0	0	48	90	03	50	50	100	3
6	PEC-II	P1LVSE2X	Professional Elective Course-II	42	0	0	48	90	03	50	50	100	3
7	PCCL	P1LVSL1	Embedded Systems lab	0	0	28	02	30	03	50	50	100	1
8	NCMC	P1PGRM	Research Methodology and IPR (Online)	Online courses (online.vtu.ac.in)									PP
								TOTAL		**350**	**350**	**700**	**20**

Professional Elective Courses (PECs): Professional Elective Courses – PEC–I and PEC–II – are common to all branches of specialization within a particular Engineering stream. Students may choose the most appropriate elective based on their field of specialization and academic requirements. *Note: The number of courses listed under each PEC group may exceed four, depending on the specializations under one stream.*

Integrated Professional Core Courses (IPCC):

The 1Mxx104x Group comprises specialization-specific core courses that are integrated with a practical component, ensuring application-oriented learning aligned with industry and research needs. The number of courses in the group depends on the number of specializations offered under a particular engineering stream.

Professional Elective Courses-I			Professional Elective Courses-II	
Code	**Title of the Course**		**Code**	**Title of the Course**
P1LVSE11	Digital System Design using Verilog HDL		P1LVSE21	Data Structures
P1LVSE12	VLSI Design Automation		P1LVSE22	VLSI Testing and Verification
P1LVSE13	VLSI for Digital Signal Processing		P1LVSE23	ASIC Design

ARM Microcontroller and Applications

Contact Hours/ Week	:3+0+0(L+T+P)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours:	: 0	SEE Marks :	50
Total Practical Hours:	: 0	Course Code	P1LVS1
Course Type:	PCC	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	To impart knowledge of ARM Cortex-M4 architecture, embedded software development, interfacing of peripherals and intelligent embedded applications.

UNIT I
Introduction to ARM Cortex-M4 Architecture: Microprocessors and Microcontrollers, Von-Neumann and Harvard Architectures, ARM Processor Family Overview, ARM Cortex-M3 and Cortex-M4 Architecture, Features of Cortex-M4: DSP Instructions, Floating Point Unit (FPU), Programmer's Model, Registers and Program Status Registers, Pipelining and Memory System, CMSIS Overview, Memory Map of Cortex-M4 based Microcontrollers (STM32 Nucleo)
8 Hours

UNIT II
Embedded Software Development and GPIO Interfacing: Embedded Software Development Flow, STM32CubeIDE Overview, Embedded C Programming for ARM Cortex-M4, Register-level vs HAL Programming, GPIO Configuration and Programming, Digital Input/Output Interfacing, Interfacing: LEDs Switches, Push Buttons, C Programming Examples
8 Hours

UNIT III
ARM Instruction Set and Peripheral Interfacing: ARM Cortex-M4 Instruction Set- Arithmetic and Logical Instructions, Memory Access Instructions, Program Flow Control Instructions, Shift and Rotate Instructions, ARM Assembler Directives, Assembly/C Programming Examples, Interfacing: 7-Segment Display, Matrix Keypad.
9 Hours

UNIT IV
Exceptions Interrupts: Exception and interrupt handling, exception model of Cortex-M4, vector table organization, Nested Vectored Interrupt Controller (NVIC), interrupt prioritization and latency, exception handling in C, fault exceptions and debugging (Hard Fault, Bus Fault, Memory

Management Fault), SysTick timer, timer-based interrupt programming, DMA architecture and DMA-based data transfer, clock configuration and power management basics, OLED/LCD Display,C Programming Examples and Embedded C Programs.
9 Hours

UNIT V
Embedded Applications using Cortex-M4: Configuration and programming of PWM, ADC, UART, SPI and I2C peripherals, advanced timer applications (input capture and output compare), DSP instruction set extensions in Cortex-M4, fixed-point and floating-point computations using FPU, FIR and IIR filter implementation using CMSIS-DSP libraries, memory optimization techniques, peripheral driver development concepts, sensor fusion fundamentals.
8 Hours

TEXT BOOKS		
1	Joseph Yiu	The Definitive guide to ARM Cortex M3 and Cortex M4 processor, Elsevier, 3rd Edition, 2013.
2	Trevor Martin,	The Designer's Guide to the Cortex-M Processor Family, Elsevier, 2nd Edition.
3	Carmine Noviello	Mastering STM32, Leanpub,

REFERENCE BOOKS		
1	Yifeng Zhu	Programming and peripheral interfacing.
2	Yifeng Zhu	Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C, E-Man Press, 5th Edition

E-resources and Manuals	
1	https://www.st.com/en/development-tools/stm32cubeide.html
2	https://arm-software.github.io/CMSIS_6/latest/General/index.html
3	https://docs.edgeimpulse.com/docs
4	Cortex-M Technical Reference Manual. revision r1p1
5	STM32F446 Reference Manual and Datasheet.

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Describe** ARM Cortex-M4 architecture and embedded programming model
CO2	**Develop** Embedded C and assembly programs for Cortex-M4 microcontrollers
CO3	**Interface** sensors and peripheral devices using on-chip peripherals.
CO4	**Develop** interrupt-driven embedded applications.
CO5	**Implement** intelligent embedded applications using TinyML concepts.

Machine Learning for Electronics Engineers

Contact Hours/ Week	:3+0+0(L+T+P)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours:	: 0	SEE Marks :	50
Total Practical Hours:	: 0	Course Code	P1LVS2
Course Type:	PCC	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	Enable students to implement machine learning methods for solving problems in electronics and embedded systems.

UNIT I
Introduction to Machine Learning and Data Analytics: Introduction to Artificial Intelligence, Machine Learning and Deep Learning. Machine learning workflow including data collection, preprocessing, feature engineering, model training, validation and testing. Supervised, unsupervised and reinforcement learning paradigms. Performance metrics accuracy, precision, recall, F1-score and confusion matrix. Feature extraction and dimensionality reduction concepts.
8 Hours

UNIT II
Supervised Learning Techniques and Applications: Linear regression, multiple regression and logistic regression. K-Nearest Neighbour (KNN), decision trees and random forests. Model evaluation techniques including bias-variance tradeoff, underfitting, overfitting and cross-validation. Sensor data classification, battery health prediction in embedded systems.
8 Hours

UNIT III
Unsupervised Learning and Pattern Discovery: Clustering techniques including K-Means and hierarchical clustering. Principal Component Analysis (PCA), anomaly detection, feature selection and data visualization methods. Sensor fault detection. ECG anomaly detection.
9 Hours

UNIT IV
Neural Networks and Deep Learning: Biological neuron model, perceptron, multilayer feedforward networks and backpropagation algorithm. Activation functions and introduction to deep learning.

Convolutional Neural Networks (CNN) and model optimization techniques. Object detection and gesture recognition in embedded vision.
9 Hours

UNIT V
Intelligent Edge AI Systems and AI-Driven Electronics Design: Embedded machine learning and TinyML concepts. Model compression techniques including quantization and pruning. TensorFlow Lite and edge AI architectures. Hardware acceleration using FPGA-based AI, AI accelerators, and TPU concepts. Introduction to AI-assisted Electronic Design Automation (EDA) including placement and routing. Emerging trends such as neuromorphic computing and AI-enabled System-on-Chip (SoC) design. Applications in AI-enabled embedded systems.
8 Hours

TEXT BOOKS		
1	Aurélien Géron	*Hands-On Machine Learning with Scikit-Learn, Keras and TensorFlow*, O'Reilly Media, 3rd Edition, 2022.
2	Christopher M. Bishop	*Pattern Recognition and Machine Learning*, Springer, 1st Edition, 2006.

REFERENCE BOOKS		
1	Ian Goodfellow, Yoshua Bengio and Aaron Courville	Deep Learning, MIT Press, 2016.
2	Wayne Wolf	Computers as Components: Principles of Embedded Computing System Design, Morgan Kaufmann, 4th Edition, 2016.
3	Pete Warden and Daniel Situnayake	TinyML: Machine Learning with TensorFlow Lite on Arduino and Ultra-Low-Power Microcontrollers, *O'Reilly Media, 1st Edition, 2019.*
4	Stuart Russell and Peter Norvig	Artificial Intelligence: A Modern Approach, *Pearson, 4th Edition, 2021.*

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Apply** machine learning concepts and performance metrics to engineering datasets.
CO2	**Analyze** supervised learning algorithms for prediction and classification problems.
CO3	**Apply** unsupervised learning techniques for pattern discovery and anomaly detection.
CO4	**Apply** neural network and deep learning models for electronics applications.
CO5	**Analyze** emerging trends such as neuromorphic computing and AI-enabled SoCs for future electronics systems.

Analog ICs Design

Contact Hours/ Week	:3+0+0(L+T+P)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours:	: 0	SEE Marks :	50
Total Practical Hours:	: 0	Course Code	P1LVS3
Course Type:	PCC	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	To impart the knowledge of Analog CMOS IC design for different amplifier topologies.

UNIT I
Introduction: Introduction to Analog IC design, General concepts- Levels of abstraction, Robustness in Analog design, MOS structure, MOS under external bias, MOSFET: Structure, Threshold voltage, I/V Characteristics, Capacitance. Small signal model. **Single stage amplifiers:** Common source stage – with resistive load, Diode connected load, current source load, Triode load, Source degeneration. Source follower, Common gate stage, Cascode stage
9 Hours

UNIT II
Differential amplifiers: Single ended differential operation, Basic differential pair, common mode response, Differential pair with MOS loads, Current mirrors: Basic current mirrors, Cascode current mirrors, Active current mirrors**.** Wide Swing Cascode Current Mirrors, Low Voltage Current Mirrors
8 Hours

UNIT III
Frequency response of amplifiers: Miller effect, Association of poles with nodes, CS-stage, Source followers, CG-stage. Feedback: General feedback considerations, Feedback topologies. Two port network models.Stability and Frequency Compensation: General considerations, Multipole systems, Phase margin, Frequency compensation **Oscillators:** Ring Oscillator, LC Oscillator
9 Hours

UNIT IV
Operational Amplifier: General considerations, one-stage OP Amps, Two-Stage op-amps, Common mode feedback, input range limitations, slew rate, power supply rejection. Design of buffer stage, Operational

Transconductance Amplifier (OTA), Gain boosting, Common-mode feedback (CMFB), Op-Amp compensation for stability, compensation of two stage op-amps. **PLL and VCO**: PLL Basics, Charge Pump PLL.
8 Hours

UNIT V
Data Converters: Data Converter Architectures: DACs, DAC specifications, R-2R ladder DAC, Charge-scaling DAC, Cyclic DAC, Pipeline DAC **Analog & Digital Converters:** ADC specifications, Successive Approximation ADC (SAR), Integrating ADC and Flash ADC
8 Hours

TEXT BOOKS:		
1	Behzad Razavi	Design of Analog CMOS Integrated Circuits 2nd Edition, McGraw Hill Education Private Limited, 2017.
2	Gayakwad, R. A., & Rekha, S	Op-Amps and Linear Integrated Circuits, 4th Edition, Pearson Education, 2021.

REFERENCE BOOKS:		
1	Adel Sedra and Kenneth C. Smith	Microelectronic Circuits Theory and Applications 8th Edition, Oxford University Press, 2020.
2	P.R. Gray; P.J. Hurst; S.H. Lewis; R.G. Meyer	Analysis and Design of Analog Integrated circuits, 6th Edition, John Wiley & Sons, 2024.

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Analyze** MOSFET characteristics and design basic single-stage CMOS amplifiers using appropriate device models
CO2	**Design** MOS differential amplifiers and current mirror circuits, and low-voltage current mirrors for analog integrated circuit applications
CO3	**Design** CMOS amplifiers and oscillators by applying frequency response analysis, feedback theory, stability criteria to achieve desired analog circuit performance
CO4	**Design** operational amplifiers, OTAs, and PLL-based circuits for analog integrated circuit applications.
CO5	**Analyze** DAC and ADC architectures by evaluating their specifications, operating principles, and performance trade-offs for mixed-signal integrated circuit applications

VLSI Design

Contact Hours/ Week	:3+0+2(L+T+P)	Credits :	4.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours:	: 0	SEE Marks :	50
Total Practical Hours:	:28	Course Code	P1LVSI4
Course Type:	IPCC	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	This course enables the students to analyze and design combinational, sequential, memory and BiCMOS circuits.

UNIT I
Introduction: MOS Structure, MOS system under External Bias, Structure and operation of the MOSFET, MOSFET Current-Voltage Characteristics, Non ideal I-V Effects - Mobility degradation, velocity saturation, Channel length modulation, Threshold voltage effects, Junction Leakage, Body Effect, Tunneling, MOSFET Capacitance **MOS Inverters- Static Characteristics:** Introduction, Resistive-Load Inverter.
8 Hours

UNIT II
Combinational Logic Circuits: Static CMOS inverter, Static behaviour, Propagation delay, Power dissipation, Pseudo NMOS inverter, Static CMOS design, Pass gates, CMOS Transmission Gates, Dynamic CMOS design. Driving Large capacitance.
8 Hours

UNIT III
Sequential Logic Circuits: Timing metrics for sequential circuits, Static latches and Registers: The Bi-stability principle, Multiplexer based Latches, Master slave edge triggered registers, Static SR Flip-Flops. Dynamic Latches and Registers: Dynamic Transmission gate Edge triggered registers, C^2MOS, True Single Phase Clock Registers (TSPCR).
8 Hours

UNIT IV
Arithmetic Building blocks: Adders, Multipliers, Barrel shifter. **Semiconductor Memories:** Memory Classification, Non-Volatile Memory devices. Read-Only Memory (ROM) Circuits,
9 Hours

UNIT V
Semiconductor Memories contd.. : Static Read-Write Memory (SRAM) Circuits, Dynamic Read-Write Memory (DRAM) Circuits **BiCMOS Logic Circuits:** Introduction, Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications. **Chip Input and Output (I/O) Circuits:** Introduction, ESD Protection, Input Circuits, Output Circuits and L (di/dt) Noise, On-Chip Clock Generation and Distribution.
9 Hours

TEXT BOOKS:		
1	Jan M Rabaey, Anantha Chandrakasan, Borivoje Nikolic	Digital Integrated Circuit A Design Perspective, 2nd Edition, PHI, 2016.
2	Sung Mo Kang & YosufLeblebici,	CMOS Digital Integrated Circuits: Analysis and Design, 41th Edition, Tata McGraw-Hill, 2002

REFERENCE BOOKS:		
1	Neil Weste and K. Eshragian,	Principles of CMOS VLSI Design: A System Perspective, 2nd Edition, Pearson Education (Asia) Pvt. Ltd. 2000.
2	Adel Sedra and Kenneth C. Smith	Microelectronic Circuits Theory and Applications 7th Edition, Oxford Higher Education, 2017.

Practical only for CIE	
1	Characterization of NMOS transistor.
2	Design the following static CMOS gates a. Inverter b. 2-input NAND c. 2-input NOR d. 2-input XOR e. 2-input XNOR. **Design (Schematic and Layout) and simulate the following circuits using Mentor graphics or Cadence for the given specifications.**
3	Design the following gates using transmission gate style, Pass transistor style and Dynamic gates style. a. Inverter b. 2-input NAND c. 2-input NOR d. 2-input XOR 2-input XNOR.

4	Design a Static CMOS D-register.
5	Design a Static CMOS Full Adder.
6	Design SRAM.
7	Design Dynamic D-registers.

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Analyze** the MOS structure, non-ideal effects and inverter characteristics
CO2	**Design** combinational circuits with different design styles.
CO3	**Design** sequential circuits with different design styles.
CO4	**Design** arithmetic building blocks and Non-Volatile Memory cells.
CO5	**Design** Volatile Memory circuits, BiCMOS circuits & Chip I/O circuits.

PROFESSIONAL ELECTIVE-I

Digital System Design Using Verilog HDL

Contact Hours/ Week	:3+0+0(L+T+P)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours:	: 0	SEE Marks :	50
Total Practical Hours:	: 0	Course Code	P1LVSE11
Course Type:	PEC	Exam Hours:	3

Course objectives: This course will enable students to:	
1.	To study Verilog HDL-based design methodologies to create synthesizable RTL designs for FPGA implementations.

UNIT I
Introduction to HDL based Digital Design: Design flow and Design styles for digital circuits, Verilog operators, Verilog Primitives, Gate level, Data flow and Behavioral modeling. Delay models, Control statements, Tasks and Functions. Synthesizable vs non-synthesizable RTL, **Introduction to SystemVerilog**: always_comb, always_ff, logic datatype, enum state machines . **RTL Testbench architecture & basics:** Directed and random testing, Self-checking testbench, waveform debugging.
9 Hours

UNIT II
Programmable Logic Devices: ROM, PAL, PLA, CPLD, FPGA, FPGA Architecture, FPGA- CLBs, switch Matrix and IOB, Configurable Logic Blocks (CLBs) in Xilinx FPGA –XC3000 and Xilinx Spartan-7, FPGA Design Flow. FPGA architectures and its usage in embedded Systems: Zynq Ultrascale + MPSoC device architecture. Introduction to Ultrascale Architectecture, System block diagram, High speed serial IO, MIO and EMIO, Functional units and peripherals, Signals interfaces and pins, On chip memory, DMA controller, Reset system, PL peripherals, Vivado design flow, Logic design on Ultrascale + MPSoC FPGA on PL block. Programming and debugging using SDK. FPGA acceleration for AI, CNN accelerator basics, Matrix multiplication accelerator, Edge AI overview.
8 Hours

UNIT III
Fixed and Floating point Arithmetic: Fixed point number system and floating point number system, Arithmetic operation on Fixed and Floating point numbers. Combinational circuit design using Verilog:Ripple Carry adder, Comparators, Combinational Multiplier – Array Multiplier, Unsigned and Signed integer multiplication, Barrel shifter, Tri-State Combinational Circuits, AXI interconnect.
8 Hours

UNIT IV
Sequential Circuit Design using Verilog: Latches, Flip Flops, Shift registers, Counters/ Timers/ Clock Dividers using T Flip Flops, Clock Dividers using D Flip Flops, Synchronous sequential Circuit Design using D and JK Flip Flops. Finite State Machines (FSM): Finite State Machines and controllers, State diagram, designing FSM using state graph, one-hot-state assignment, controller design. Traffic Light control system. Mealy vs Moore optimization, FSM encoding optimization.
9 Hours

UNIT V
Designing Data path components and Memory units: Serial adder, multiplier using Shift and Add, Fixed point and, Binary Divider, Accumulator, Booth Multiplier, Multiply and Accumulate (MAC) unit, Floating point Multiplier. Memory Design – FIFO, Stack, Circular Buffer.
8 Hours

TEXT BOOKS:		
1	Frank Vahid	Digital Design with RTL Design, VHDL, and Verilog 2nd, Edition John Wiley and SonsPublishers, 2011.
2	Samir Palnitkar	Verilog HDL A guide to Digital Design and Synthesis 2nd Edition, Pearson Education, 2017.
3	Reference Manual	Zynq UltraScale+ Device Technical Reference Manual.

REFERENCE BOOKS:		
1	Pong P. C	FPGA Prototyping by Verilog Examples, Wiley India Pvt. Ltd., 2008.
2	Stuart Sutherland, Simon Davidmann and Peter Flake	SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling, 2nd Edition, Springer, 2006.
3	Wayne Wolf	FPGA-Based System Design, Pearson Education, 2004.

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Design** digital systems using Verilog/System Verilog HDL through RTL modeling, simulation, verification, and testbench development.
CO2	**Implement** digital, embedded, and AI accelerator systems using PLDs and FPGA technologies.
CO3	**Design** fixed- and floating-point arithmetic units, combinational circuits, and AXI-based digital systems using Verilog HDL.
CO4	**Design** sequential circuits and FSM-based controllers using Verilog HDL
CO5	**Design** datapath components, multipliers, dividers, and memory units using Verilog HDL.

VLSI Design Automation

Contact Hours/ Week	:3+0+0(L+T+P)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours:	: 0	SEE Marks :	50
Total Practical Hours:	: 0	Course Code	P1LVSE12
Course Type:	PEC	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	To impart knowledge on implementation of automation methods for VLSI physical design.

UNIT I
Logic Synthesis & Verification: Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis. **VLSI Automation Algorithms**: Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.
9 Hours

UNIT II
Placement, Floor Planning & Pin Assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment**.**
8 Hours

UNIT III
Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches.
8 Hours

UNIT IV
Detailed Routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms. **Over The Cell Routing & Via Minimization**: two layers over the cell routers, constrained & unconstrained via minimization.
8 Hours

UNIT V
Scripting Languages: Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables. Inter process Communication Threads, Compilation & Line Interfacing.
9 Hours

TEXT BOOKS		
1	NaveedShervani	Algorithms for VLSI physical design Automation, Kluwer Academic Publisher, 3rd Edition, 2016
2	ChristophnMeinel & Thorsten Theobold	Algorithm and Data Structures for VLSI Design, KAP, 2016.

REFERENCE BOOKS:		
1	Rolf Drechsheler	Evolutionary Algorithm for VLSI, Springer, 2nd Edition, 2016.
2	Randal L, Schwartz Tom Phoenix	Learning PERL, Oreilly Publications, 8th Edition, 2021.

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Analyze** partitioning algorithms, high-level synthesis techniques, and hardware model verification methods used in VLSI design automation.
CO2	**Analyze** placement, floor planning, and pin assignment algorithms to optimize layout design and routing efficiency.
CO3	**Develop** routing algorithms for VLSI interconnect design.
CO4	**Analyze** multilayer routing algorithms and their impact on VLSI physical design
CO5	**Develop** scripts for automating VLSI design tasks and workflows.

VLSI for Digital Signal Processing

Contact Hours/ Week	:3+0+0(L+T+P)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours:	: 0	SEE Marks :	50
Total Practical Hours:	: 0	Course Code	P1LVSE13
Course Type:	PEC	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	To study custom or semi-custom VLSI circuits for Signal Processing applications.

UNIT I
Introduction: DSP algorithms: FIR and IIR Filters, Representation of DSP Algorithms. **Iteration Bounds:** loop bound and Iteration bound, Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs.
9 Hours

UNIT II
Pipelining and parallel processing: pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power. **Retiming:** Properties, Solving Systems of Inequalities, Retiming techniques.
8 Hours

UNIT III
Unfolding: Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Applications of Unfolding in FIR filters, IIR filters, FFT processors, DSP accelerators.
8 Hours

UNIT IV
Systolic architecture design: systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design.
8 Hours

UNIT V
Fast convolution–Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, **Pipelined and Parallel recursive filter:** Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing.
9 Hours

TEXT BOOK		
1	Keshab K.Parhi	"VLSI Digital Signal Processing systems, Design and implementation ", Wiley, Inter Science, 1999.

REFERENCE BOOKS:		
1	Mohammed Isamail and Terri Fiez	Analog VLSI Signal and Information Processing, Mc Graw-Hill, 1994.
2	Jose E. France, YannisTsividis	Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing, Prentice Hall, 2nd Edition, 1994.

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Develop** DSP algorithms using block diagrams, signal flow graphs and data flow graphs.
CO2	**Compute** the iteration bound critical path, power consumption in filters.
CO3	**Perform** retiming in filters and unfolding.
CO4	**Analyze** Systolic architecture design methodologies
CO5	**Perform** efficient implementation of filters using pipelining and parallel processing

PROFESSIONAL ELECTIVE-II

Data Structures

Contact Hours/ Week	:3+0+0(L+T+P)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours:	: 0	SEE Marks :	50
Total Practical Hours:	: 0	Course Code	P1LVSE21
Course Type:	PEC	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	Enable students to learn implementation of different data structures.

UNIT I
Structures and Unions: Defining a Structure, declaring Structure variables, accessing Structure members, Structure initialization, copying and comparing Structure variables, and operations on individual members, array of Structures, array within Structure, Structure within Structure, Structures and Functions, Unions, size of structures. File management in C: Defining and Opening a file, Closing a file, Input/output operations on files - getc(), putc(), getw(), putw(), fscanf(), fprintf(), Error handling during I/O operations - feof(), ferror(), Random access to files - ftell(), rewind(), fseek(), Command line arguments.
9 Hours

UNIT II
Stack: Definition and Examples, representing Stacks in C, Example: Infix, Postfix, and Prefix. **Recursion:** Recursive Definition and Processes, Recursion in C. **Queues:** The Queue and Its Sequential Representation: C implementation of Queues, Insertion, Deletion and Display operations, Types of Queues (Linear and Circular Queues) Self-Study: Priority and Double Ended Queues.
8 Hours

UNIT III
Dynamic memory allocation: malloc(), calloc(), realloc(), free(). **Linked lists:** Inserting and removing nodes from a list, linked implementation of stacks, getnode and freenode operations, linked implementation of queues, examples of list operation, list implementation of priority queues, header nodes.

Lists in C: allocating and freeing dynamic variables, linked lists using dynamic variables, queues as lists in C, examples of list operations in C, non-integer and non-homogeneous lists, implementing header nodes.
8 Hours

UNIT IV
Circular and Doubly Linked Lists: Circular lists, stack as a circular list, queue as a circular list, primitive operations on circular lists, doubly linked lists, Primitive operations on doubly linked list.
8 Hours

UNIT V
Trees: Operations on Binary Trees, Applications of Binary Trees, and Binary Tree Representations: Node representation of Binary Trees, Internal and External Nodes, Implicit array representation of Binary Trees, Binary Tree Traversals in C. Trees and Their applications: C Representations of Trees, Tree Traversals, General Expressions as Trees, Evaluating an Expression Tree, Constructing a Tree.
9 Hours

Text Books:		
1	Yashavant Kanetkar	Data Structures Through C, BPB publications, 4th Edition, 2022.
2	E. Balagurusamy	Programming in ANSI C, 3rd Edition, TMH, 2018.
3	Yedidyah Langsam, Moshe J. Augenstein, Aaron M. Tenenbaum	Data structures using C and C++, PHI, 2nd Edition, 2015.

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Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Apply** advanced C programming techniques to develop solutions for a given problem
CO2	**Implement** different linear data structures using static memory allocation technique
CO3	**Implement** different types of linked lists by using dynamic memory allocation technique
CO4	**Implement** non-linear data structures by using dynamic memory allocation technique.
CO5	**Apply** the knowledge of stacks, queues, linked lists and trees for developing solutions to given problems

VLSI Testing and Verification

Contact Hours/ Week	:3+0+0(L+T+P)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours:	: 0	SEE Marks :	50
Total Practical Hours:	: 0	Course Code	P1LVSE22
Course Type:	PEC	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	Understand fault models, test generation techniques, and verification methodologies used for testing and validating VLSI systems.

UNIT I
Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing. **Faults:** Single Stuck at faults, Temporary Faults. Bridging faults, Transient faults. **Fault modeling:** Fault equivalence, dominance and collapsing. **Fault Simulation:** parallel, concurrent and deductive simulation.
9 Hours

UNIT II
Test Generation for Combinational Logic Circuits: Test Generation Techniques for Combinational Circuits: Truth table method, Fault matrix method, Boolean difference method, Path sensitization method, D-Roth algorithm, PODEM and FAN. Detection of Multiple Faults in Combinational Logic Circuits
8 Hours

UNIT III
Design of Testable Sequential Circuits: Controllability and Observability, Ad Hoc Design Rules for Improving Testability, The Scan-Path Technique for Testable Sequential Circuit Design, Level-Sensitive Scan Design, Random Access Scan Technique, Partial Scan, Testable Sequential Circuit Design Using Nonscan Techniques, Crosscheck, Boundary Scan.
8 Hours

UNIT IV
Built-In Self Test: Test Pattern Generation for BIST, Output Response Analysis, BIST Architectures-BILBO. **Testable Memory Design:** RAM Fault Models, Test Algorithms for RAMs: March algorithm(Row, Column), galloping algorithm, butterfly

algorithm, Neighbourhood Pattern Sensitive Faults(NPSF), Detection of Pattern Sensitive Faults, BIST Techniques for Ram Chips, Test Generation and BIST for Embedded RAMs.
8 Hours

UNIT V
Importance of Design Verification: The importance of verification, Reconvergence model, Formal verification, Assertion based verification, Equivalence checking, model checking, and functional verification. **Verification Tools:** Linting tools: Limitations of linting tools, lintingverilog source code, linting VHDL source code, lintingOpenVera and e-source code, code reviews. **Simulators:** Stimulus and response, Event based simulation, cycle based simulation, Co-simulators, verification intellectual property: hardware modelers, waveform viewers. **Verification plan:** The role of verification plan: specifying the verification plan, Levels of verification: unit level verification, reusable components verification, ASIC and FPGA verification, system level verification, board level verification.
9 Hours

Text Books:		
1	P. K. Lala	Digital Circuit Testing and Testability, Academic Press, 1997.
2	M.L. Bushnell and V.D. Agrawal	Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Springer, 1st Corrected Edition 2002, Corr. 2nd printing 2004.

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Analyze** fault models and fault simulation techniques used in VLSI testing.
CO2	**Apply** test generation techniques and algorithms for fault detection in combinational logic circuits.
CO3	**Apply** design-for-testability techniques to improve the testability of sequential circuits
CO4	**Analyze** BIST architectures and memory testing algorithms for fault detection in VLSI systems
CO5	**Analyze** verification methodologies, tools, and plans for VLSI systems.

ASIC Design

Contact Hours/ Week	:3+0+0(L+T+P)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours:	: 0	SEE Marks :	50
Total Practical Hours:	: 0	Course Code	P1LVSE23
Course Type:	PEC	Exam Hours:	3

Course objectives: This course will enable students to:	
1.	To understand ASIC design methodologies, programmable ASIC architectures, memory technologies, and CAD-based techniques used in ASIC design, synthesis, and implementation.

UNIT I
Introduction: ASIC Design Methodology, Full Custom, Semi-Custom and Programmable ASICs, ASIC Design Flow with examples, FPGA Design Flow with examples, ASIC vs FPGA Design, ASIC Cell Libraries and Standard Cells.
9 Hours

UNIT II
Data Logic Cells: Datapath Elements, Adders and Multipliers, Arithmetic Logic Units (ALU), Low Power Datapath: Design Logical Effort and Delay Optimization, Area, Power and Performance Trade-offs. Standard Cell Library Design.
8 Hours

UNIT III
Low-Level Design Entry: Schematic Entry, **Programmable ASIC**: Anti-fuse, Static RAM, EPROM and EEPROM Technology, FPGA, Programmable ASIC logic cells, ASIC I/O cells, Programmable ASIC Interconnects
8 Hours

UNIT IV
Low Level Design Language: introduction to EDIF, PLA Tools and CFI designs representation. Half gate ASIC. Introduction to Synthesis and Simulation. **ASIC Construction:** Physical Design, CAD Tools, System Partitioning, Estimate ASIC size, FPGA Partitioning and its Methods.
8 Hours

UNIT V
Floor Planning, Placement and Routing: Physical Design, System Partitioning, Estimating ASIC size, partitioning methods. Floor planning tools, I/O and power planning, clock planning, placement algorithms. Global Routing, Local Routing, Detail Routing, Special Routing, Circuit Extraction and DRC.
9 Hours

TEXT BOOKS:		
1	M.J.S .Smith	"Application - Specific Integrated Circuits" – Pearson Education, 2010.
2	Jose E.France, YannisTsividis	"Design of Analog-Digital VLSI Circuits for Telecommunication and signal processing", 2nd Edition, Prentice Hall, 1993.
3	MalcolmR.Haskard; Lan. C. May	"Analog VLSI Design – NMOS and CMOS", Prentice Hall, 1998.
4	Mohammed Ismail and Terri Fiez	"Analog VLSI Signal and Information Processing", McGraw Hill, 1994.

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Analyze** ASIC architectures, design methodologies, and ASIC–FPGA design flows
CO2	**Apply** optimization techniques for datapath and arithmetic components in ASIC design.
CO3	**Implement** programmable ASIC architectures using RTL design methodologies
CO4	**Apply** the fundamentals of ASIC and FPGA design, including design representation, synthesis, simulation, physical design, and partitioning techniques
CO5	**Develop** physical implementation solutions using floor planning, partitioning, placement, routing, and verification techniques.

Embedded Systems Lab

Contact Hours/ Week:	0+0+2 (L+T+P)	Credits:	1
Total Lecture Hours:	0	CIE Marks:	50
Total Tutorial Hours:	0	SEE Marks:	50
Total Practical Hours:	28	Course Code:	P1LVSL1
Course Type:	Practical (PCCL)	Exam Hours:	3

Course objectives: This course will enable students to:	
1.	To develop embedded applications using ARM Cortex-M4 microcontrollers, peripheral interfacing, RTOS concepts and TinyML-based intelligent systems

Hardware Platform: STM32 Nucleo-F446RE
Sensors: IMU, Temperature/Humidity, IR/Proximity, Motor Driver Modules.

List of Lab Experiments	
1.	Develop a system to implement a calculator capable of performing arithmetic and logical operations using a 4×4 matrix keypad and 16×2 LCD interfaced to STM32 Cortex-M4 microcontroller.
2.	Develop a traffic control system using on-chip timers and LEDs/7-segment displays interfaced to STM32 Cortex-M4 microcontroller.
3.	Develop a temperature monitoring and control system using a temperature sensor, ADC, LCD and relay interfaced to STM32 Cortex-M4 microcontroller.
4.	Develop a system to measure and control the speed of a DC motor using PWM and timer modules of STM32 Cortex-M4 microcontroller.
5.	Develop a system to control the direction and speed of a stepper motor using push buttons interfaced to STM32 Cortex-M4 microcontroller.
6.	Develop a system to measure the frequency of an external signal or rotational speed of a motor using timer input capture mode.
7.	Develop a bottle filling control system using IR/Proximity sensors, stepper motor and actuator control.
8.	Develop a multi-floor elevator control system using push buttons, proximity sensors, motor control and display modules.
9	Develop a digital weighing machine using load cell, instrumentation amplifier, ADC and LCD interfaced to STM32 Cortex-M4.
10	Develop a real-time clock using STM32 timers/RTC peripheral and display date-time information on LCD.

Open ended experiments (only for CIE):	
1.	Implement FIR and IIR filters using CMSIS-DSP libraries and Cortex-M4 DSP instructions for real-time signal processing.
2.	IMU Sensor Data Acquisition and Visualization
3.	Develop a real-time signal spectrum analyzer using ADC sampling and Fast Fourier Transform (FFT) on STM32 Cortex-M4.

Suggested Software Tools: STM32CubeIDE,

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Develop** embedded applications using STM32 Cortex-M4 CMOS RF Circuit Design microcontrollers and Embedded C programming techniques.
CO2	**Apply** peripheral interfacing techniques for integrating sensors, actuators, displays, timers, ADCs, and communication modules in embedded systems.
CO3	**Design** and implement real-time monitoring and control systems using STM32 Cortex-M4 based embedded platforms.

2nd Semester

Design of Intelligent IoT Systems

Contact Hours/ Week:	3+0+2 (L+T+P)	Credits:	4.0
Total Lecture Hours:	42	CIE Marks:	50
Total Tutorial Hours:	0	SEE Marks:	50
Total Practical Hours:	28	Course Code:	
Course Type:	IPCC	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	To understand modern IoT architectures, embedded connectivity, edge computing, IoT analytics and AI-enabled IoT systems.

UNIT I
Fundamentals of IoT and System Architecture: Definition and Characteristics of IoT, IoT Architectures and Reference Models, IoT Functional Stack, Data Management and Compute Stack, Communication Models and APIs, IoT Framework, Types of IoT Systems, Challenges in IoT System Design, IoT Design Methodology, IoT Levels and Deployment Templates, Introduction to Edge, Fog and Cloud Computing
8 Hours

UNIT II
IoT Devices, Sensors and Embedded Platforms: Introduction to STM32, Arduino and Raspberry Pi Platforms, Embedded IoT Nodes and Gateways, Sensors and Actuators for IoT Applications, Smart Sensors and Smart Objects, Sensor Interfacing Techniques, Actuator Interfacing, Power Management in IoT Devices, IoT Device Design Considerations.
8 Hours

UNIT III
IoT Connectivity and Communication Protocols: IoT Connectivity Technologies: IEEE 802.15.4, Zigbee, Thread, RFID, NFC, LoRaWAN, Sigfox, NB-IoT, Wi-Fi and Bluetooth Low Energy (BLE). IoT Communication Protocols: IPv6 and 6LoWPAN, MQTT and MQTT-SN, CoAP, RESTful APIs, WebSocket Communication, Device-to-Device, Device-to-Gateway and Device-to-Cloud Communication Models, IoT Gateway Architecture
8 Hours

UNIT IV
Edge Computing and IoT Data Management: Edge Computing Concepts and Architecture, Fog Computing Fundamentals, IoT Edge Devices and Gateways, Edge Analytics and Distributed Intelligence, IoT Data Acquisition and Pre-processing, Sensor Data Management, Message Queuing Telemetry Transport (MQTT), Constrained Application Protocol (CoAP), Advanced IoT Communication Architectures, Cloud Integration for IoT Systems, Device Management and Over-the-Air (OTA) Updates, Data Storage and Visualization Platforms for IoT Applications.
9 Hours

UNIT V
Secure and Industrial IoT Applications: IoT Security Fundamentals, Threats and Vulnerabilities in IoT Systems, Lightweight Authentication and Authorization, Cryptographic Techniques for Resource-Constrained Devices, Secure Communication Protocols, Device Identity and Access Management. Introduction to AIoT, AI-enabled Sensor Analytics, Intelligent Event Detection and Predictive Monitoring. Case Studies: Smart Healthcare Systems, Industrial IoT and Industry 4.0, Smart Agriculture, Smart Energy Monitoring, Connected and Wearable Devices.
9 Hours

TEXT BOOKS:		
1	Misra S., Mukherjee A., Roy A	Introduction to IoT", Cambridge University Press, 2021.
2	David Hanes, Gonzalo Salgueiro, et al	IoT Fundamentals, Cisco Press
3	Arshdeep Bahga and Vijay Madisetti	Internet of Things: A Hands-On Approach

REFERENCE BOOKS		
1	Adrian McEwen, Hakim Cassimally	Designing the Internet of Things, John Wiley & Sons Ltd, 1st Edition, 2013
2.	Brian Russell, Drew Van Duren	Practical Internet of Things Security, Packt Publishing, 1st Edition, 2016
3.	Dieter Uckelmann Mark Harrison Florian Michahelles	Architecting the Internet of Things, Springer, 1st Edition, 2013

IOT Lab Experiments	
1.	Develop an STM32-based IoT node for acquisition of temperature and humidity data using digital sensors and serial monitoring.
2.	Develop an IoT gateway using Raspberry Pi for collecting sensor data from STM32 nodes.
3.	Develop a Wi-Fi enabled sensor monitoring system using STM32 and ESP8266/ESP32.
4.	Implement MQTT publish-subscribe communication between STM32 sensor node and Raspberry Pi MQTT broker.
5.	Develop a Node-RED dashboard for real-time visualization of sensor data.
6.	Implement a REST-based IoT application for remote monitoring and control of LEDs or actuators.
7.	Develop a smart environmental monitoring system using multiple sensors and cloud data logging.
8.	Develop a BLE-based IoT monitoring system using STM32 and mobile application interface.
9.	Implement edge analytics on Raspberry Pi for threshold-based event detection and alert generation.
10	Develop a secure IoT monitoring system using MQTT authentication and encrypted communication.
Open ended experiments (only for CIE):	
1	Design and implement an IoT-based smart monitoring system for a chosen application using STM32 Nucleo and/or Raspberry Pi with sensor integration, connectivity, and cloud-based visualization.
2	Design and develop a secure intelligent IoT solution incorporating edge analytics, remote monitoring, and appropriate IoT communication protocols for a real-world application

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Analyze** IoT architectures, design methodologies, and deployment models for connected systems
CO2	**Develop** embedded IoT nodes and gateways using sensors, actuators, and hardware platforms for IoT applications
CO3	**Apply** IoT communication technologies and protocols for reliable data exchange in connected IoT environments
CO4	**Analyze** edge computing and IoT data management frameworks for scalable and efficient IoT deployments
CO5	**Apply** security mechanisms and AIoT concepts in the design of intelligent IoT solutions for real-world applications.

Semiconductor Process Technology

Contact Hours/ Week	:3+0+0(L+T+P)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours:	: 0	SEE Marks :	50
Total Practical Hours:	: 0	Course Code	
Course Type:	PCC	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	This course aims at understanding the manufacturing methods and their underlying scientific principles in the context of technologies used in VLSI chip fabrication.

UNIT I
Introduction: Electronic-Grade Silicon, Czochralski Crystal Growing, Float Zone Crystal Growing, Silicon Shaping, Process Considerations. Environment for VLSI technology: clean room and safety requirements, Wafer cleaning process. **Epitaxy:** Introduction, Vapour-Phase Epitaxy, Molecular Beam Epitaxy, Epitaxial Evaluation. **Oxidation:** kinetics of silicon dioxide growth for thick, thin and ultra-thin films. Oxidation technologies in VLSI and ULSI; Characterization of oxide films.
8 Hours

UNIT II
Chemical Vapour deposition techniques: CVD (PECVD, APCVD, LPCVD and ALD) techniques for deposition of materials. **Metallization:** Metallization Applications, Metallization Choices, Physical Vapor Deposition (evaporation and sputtering techniques). Contact, Via, and Passivation, Failure mechanisms in metal interconnect; multilevel Metallization schemes.
8 Hours

UNIT III
Impurity incorporation: Models of **Diffusion** in Solids, Fick's laws for Diffusion, Measurement Techniques, Fast Diffusion in Silicon. **Ion implantation:** Introduction, Range Theory, Implantation Equipment, Annealing, Shallow Junctions, High-Energy Implantation, annealing; Characterization of impurity profiles. **Reactive Plasma Etching:** Introduction, Plasma Properties, Feature-Size Control and Anisotropic Etch Mechanisms, Other Properties of Etch Processes, Reactive Plasma-Etching Techniques and Equipment, Specific Etch Processes.
9 Hours

UNIT IV
Lithography: Introduction, Positive and Negative photoresists, Optical Lithography, Electron Lithography, X-ray Lithography, Ion Lithography. Layout Design rules, Lambda based rules. **Thin film Characterization: Overview** of thin film characterization, **Structural** properties: Optical Profiler Scanning electron microscopy (SEM), TEM, AFM, X-ray diffraction (XRD), **Electrical** properties: Resistance/resistivity – four point probe, Vander Pauw, **Mechanical** properties: Non contact optical Profiler, Stress-curvature measurements**.**
9 Hours

UNIT V
VLSI Process Integration: Introduction, Fundamental Considerations for IC Processing, NMOS IC technology, CMOS IC Technology, FF,SS, & TT processes of CMOS. MOS Memory IC Technology, Introduction to Embedded Non-Volatile Memory (eNVM) fabrication. **Packaging of VLSI Devices:** Introduction, Package Types, Packaging Design Considerations and Flip chip packaging.
8 Hours

TEXT BOOKS:		
1	S. M. Sze,	VLSI Technology, McGraw-Hill, 2nd Edition, 2017.
2	S.K. Ghandhi,	VLSI Fabrication Principles, John Wiley Inc., New York, 2nd Edition, 2008.
REFERENCE BOOKS:		
1	John A. Venables	Introduction to Surface and Thin Films Processes, Cambridge University Press, 2000.
2	Leon I. Maissel and Reinhard Glang.	Handbook of Thin Film Technology, McGraw-Hill Publishing Company, New Delhi (1970)

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Analyze** the crystal growth process and select appropriate epitaxial growth techniques for IC's fabrication
CO2	**Analyze** and Select appropriate deposition method to deposit various material in the thin film for IC's fabrication.
CO3	**Select** appropriate impurity incorporation, and etching methods used in IC's fabrication
CO4	**Describe** the various lithography techniques used in IC's fabrication. Analyze the material properties of thin films using characterization techniques
CO5	**Apply** various process sequences and special considerations for IC's fabrication. Select an appropriate package type and explain design considerations of VLSI devices

High Performance Computing Embedded Systems

Contact Hours/ Week:	3+0+0 (L+T+P)	Credits:	3.0
Total Lecture Hours:	42	CIE Marks:	50
Total Tutorial Hours:	0	SEE Marks:	50
Total Practical Hours:	0	Course Code:	
Course Type:	PCC	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	To develop the knowledge and skills required to design, optimize and implement efficient embedded computing system to meet the performance and real time constraints.

UNIT I
Basics of computer Design and performance evaluation: Computer architecture, Quantitative principles of computer design, CPU performance and its factors, SPEC Benchmarks, Abstract level of Processor, Flynn's Classification of Parallel Computers.
8 Hours

UNIT II
Computational model: Micro architecture, High performance arithmetic architectures. **Instruction Level Parallelisms:** Basic concepts, Dependencies between instructions, preserving sequential consistency. **Pipelining:** Introduction to pipelining, Instruction pipeline design, pipeline hazards, deep pipeline micro architectures, shared memory organization.
8 Hours

UNIT III
Multicore processor Architectures: Multiprocessor architectures, Processing elements, Interconnection networks **Memory systems:** Memory hierarchy, memory system performance**,** cache memory, cache coherence Cache performance issues, shared memory. High performance Bus architecture, Parallel virtual-Machine architecture and programming model.
8 Hours

UNIT IV
Real Time Embedded systems: Real time systems, Embedded system architecture. **System resources:** Resource analysis Real time service utility**,** Real-Time OS, Firmware components. **Process and Threads:** Process and thread creations, Necessary and Sufficient feasibility condition, Preemptive Fixed-Priority Policy Programs related to semaphores, message queue, shared buffer applications involving inter task/thread communication. **Introduction to Embedded co-processor**: GPU, Early GPU**,** ML Accelerator
9 Hours

UNIT V
Scheduling: FCFS, Priority, Round Robin scheduling**,** Rate Monotonic and Deadline Monotonic scheduling, Dynamic priority policies. **Debugging Components:** Exceptions, assert, Checking return codes. Single-step debugging, kernel scheduler traces, Test access ports, Trace ports, Power-On self-test and diagnostics, External test equipment, Application-level debugging. **Performance Tuning:** Basic concepts of drill-down tuning, hardware – supported profiling and tracing.
9 Hours

Text Book:		
1	Sam Siewert	"Real-Time Embedded Systems and Components" Cengage Learning India Edition, 2016.
2	KVKK Prasad	Embedded/ Real time systems, Concepts, Design and Programming, Dream Techn Press, 2010.

Reference Books:		
1	James W.S. Liu	"Real Time System", Pearson education, 2008.
2	Dream Tech software team	Programming for Embedded system, John Wiley India Pvt.Ltd, 2008
3	Abraham S ilberschatz, Peter Baer Galvin, Greg Gagne	Operating system concepts, Wiley India, 9th Edition, 2013.

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Analyze** System architecture for high performance computing.
CO2	**Analyze** the system resources required to build embedded system.
CO3	**Select** suitable memory and I/O to build embedded systems.
CO4	**Analyze** the architecture and functioning of real time embedded systems and GPUs.
CO5	**Analyze** the scheduling, debugging components, performance, communication in multithread and multi process algorithms.

Static Timing Analysis

Contact Hours/ Week:	3+0+0 (L+T+P)	Credits:	3.0
Total Lecture Hours:	42	CIE Marks:	50
Total Tutorial Hours:	0	SEE Marks:	50
Total Practical Hours:	0	Course Code:	
Course Type:	PCC	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	To study Static Timing Analysis (STA) techniques for verifying and optimizing the timing performance of digital VLSI circuits.

UNIT I
Introduction: VLSI Physical Design flow, FPGA Design Flow, Introduction to static timing analysis (STA), STA at different design phases, Limitations of STA, CMOS Logic Design: Basic MOS Structure, CMOS Logic Gate, Standard cells. Modeling of CMOS cells, Switching waveform, Propagation delay, Slew of a waveform, Skew between signals, Timing Arcs and Unateness, Min and Max Timing Paths, Clock Domains, Operating Conditions.
8 Hours

UNIT II
Standard Cell Library: Pin Capacitance, Timing modeling: Linear Timing Model, Non-Linear Delay Model, Threshold Specifications and Slew Derating. Timing models for combinational cells: Delay and Slew Models, General Combinational Block. Timing models for sequential cells: Synchronous Checks, Asynchronous Checks, Propagation Delay. State dependent models: XOR, XNOR and Sequential Cells. Power dissipation modeling, Models for Crosstalk Noise Analysis, Cell library attributes: Area Specification, Function Specification, SDF Condition. Characterization and Operating Conditions.
9 Hours

UNIT III
Interconnect Parasitics: RLC for Interconnect, Wireload Models, Representing Coupling Capacitances, Hierarchical Methodology, Block Replicated in Layout, Reducing Parasitics for Critical Nets, Reducing Interconnect Resistance, Parasitics for Correlated Nets. Delay Calculation Basics, Delay calculation with Interconnect, Pre-layout Timing, Post-layout Timing, Cell Delay using Effective Capacitance, Interconnect Delay, Elmore Delay, Higher Order Interconnect Delay Estimation, Full Chip Delay Calculation, Slew Merging, Different Voltage

Domains, Path Delay Calculation, Combinational Path Delay, Path to a Flip-flop, Input to Flip-flop Path, Flip-flop to Flip-flop Path, Multiple Paths, Slack Calculation. OCV (On-Chip Variation,) AOCV (Advanced On-Chip Variation).
9 Hours

UNIT IV
Configuring the STA Environment: STA Environment, Specifying Clocks, Generated Clocks, Example of Master Clock at Clock Gating Cell Output, Generated Clock using Edge and Edge_shift Options, Generated Clock using Invert Option, Clock Latency for Generated Clocks, Typical Clock Generation Scenario, Constraining Input Paths, Constraining Output Paths, Example A, Example B, Example C, Timing Path Groups, Modeling of External Attributes, Modeling Drive Strengths, Modeling Capacitive Load, Design Rule Checks, Virtual Clocks, Refining the Timing Analysis, Specifying Inactive Signals, Breaking Timing Arcs in Cells, Point-to-Point Specification, Path Segmentation. Crosstalk noise and delay.
8 Hours

UNIT V
Timing Verification: Setup Timing Check, Flip-flop to Flip-flop Path, Input to Flip-flop Path, Input Path with Actual Clock, Flip Flop To Output Path, Input to Output Path, Frequency Histogram, Hold Timing Check, Flip-flop to Flip-flop Path, Hold Slack Calculation, Input to Flip-flop Path, Flip-flop to Output Path, Flip-flop to Output Path with Actual Clock, Input to Output Path, Multicycle Paths, Crossing Clock Domains, False Paths, Half- Cycle Paths, Removal Timing Check, Recovery Timing Check, Timing across Clock Domains, Slow to Fast Clock Domains, Fast To Slow Clock Domains, Half-cycle Path - Case 1, Half-cycle Path -Case 2, Fast to Slow Clock Domain, Slow to Fast Clock Domain, Multiple Clocks, Integer Multiples, Non-Integer Multiples, Phase Shifted. Timing Closure and Optimization: Setup and hold violation fixing. Clock tree optimization.
9 Hours

TEXT BOOKS:		
1	J. Bhasker, R Chadha	Static Timing Analysis for Nanometer Designs: A Practical Approach, Springer 2009
2	Sridhar Gangadharan, Sanjay Churiwala	Constraining Designs for Synthesis and Timing Analysis – A Practical Guide to Synopsis Design Constraints (SDC), Springer 2013
3	Giovanni De Micheli	Synthesis and Optimization of Digital Circuits, TMH, 1994
4	R. Jayagowri and Pushpendra S. Yadav	Static Timing Analysis for VLSI circuits, MedTech Science Press,2024

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Apply** VLSI physical design flow, FPGA design flow, and Static Timing Analysis (STA) concepts for analysing the timing behaviour of digital circuits.
CO2	**Analyse** standard cell library characteristics, timing and power models, and operating conditions
CO3	**Evaluate** the impact of interconnect parasitics on delay, slew, and slack, and perform timing analysis of digital circuits using pre-layout and post-layout timing models.
CO4	**Configure** the STA environment by defining clocks, timing constraints, loads, and design rules to perform accurate timing analysis and verification.
CO5	**Perform** setup, hold, recovery, and removal timing verification, by analysing timing behavior across multiple clock domains and timing paths in digital circuits.

Professional Elective – III

Low Power VLSI Design

Contact Hours/ Week:	3+0+0 (L+T+P)	Credits:	3.0
Total Lecture Hours:	42	CIE Marks:	50
Total Tutorial Hours:	0	SEE Marks:	50
Total Practical Hours:	0	Course Code:	
Course Type:	PEC	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	This course enables students to apply low-power VLSI design techniques for minimizing power consumption in digital integrated circuits at the device, circuit, logic, and architectural levels.

UNIT I
Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices. **Device & Technology Impact on Low Power:** Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.
9 Hours

UNIT II
Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.
8 Hours

UNIT III
Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. **Low Power Design Circuit level**: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library.
8 Hours

UNIT IV
Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. **Low power Architecture & Systems:** Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.
8 Hours
UNIT V
Low power Clock Distribution, **Algorithm & Architectural Level Methodologies:** Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.
9 Hours

Text Books:		
1	Kaushik Roy, Sharat Prasad	"Low-Power CMOS VLSI Circuit Design" Wiley, 2009
2	Rabaey, Pedram	"Low Power Design Methodologies" Kluwer Academic, 2012.

Reference Books:		
1	Gary K. Yeap	"Practical Low Power Digital VLSI Design", KAP, 2012.

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Analyze** the impact of low power in VLSI circuits.
CO2	**Apply** power estimation and simulation techniques for evaluating power consumption in CMOS digital circuits
CO3	**Apply** circuit-level low-power design techniques for reducing power consumption in CMOS digital circuits
CO4	**Design** low-power logic and architectural solutions using optimization techniques for digital systems
CO5	**Develop** energy-efficient VLSI systems using algorithmic, architectural, and clock distribution methodologies

RISC V Architecture

Contact Hours/ Week:	3+0+0 (L+T+P)	Credits:	3.0
Total Lecture Hours:	42	CIE Marks:	50
Total Tutorial Hours:	0	SEE Marks:	50
Total Practical Hours:	0	Course Code:	
Course Type:	PEC	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	To impart the knowledge of RISC-V Instruction Set Architecture and its design.

UNIT I
Evolution of the RISC-V Architecture: RISC-V Base Instruction Sets and Extensions. Comparison of RISC-V, MIPS, ARM and x86 Architectures, Programmers model for RV32I, Operation and addressing modes of Data Processing instructions, Control transfer instructions, Conditional branches, Assembly level programming examples.
8 Hours

UNIT II
Data Transfer Instructions, Control and Status Register Instructions, Pseudo Instructions, Assembler directives, RISC-V Machine level instruction formats: Base Instruction formats for R, I, S/B, U/J type instructions, immediate encodings. RISC-V memory map, Compiling, Assembling, Linking and Loading RISC-V programs, Exception handlers. Assembly level programming examples.
9 Hours

UNIT III
RISC-V Microarchitecture design: Architectural state and Instruction set, Design process, Performance analysis, Single cycle processor design: Single cycle data-path and control. Multi-cycle processor design: Multi-cycle data-path and control. Pipelined processor design:
9 Hours

UNIT IV
HDL representation of Single cycle processor: Controller, Main decoder, ALU decoder, Resettable flip-flop with enable, Data path, Extend unit, Multiplexers, Test bench, Top level module, Instruction memory and data memory.
8 Hours

UNIT V
Pipelined processor data-path and control. Hazards, Branch predictions, Super Scalar processors, out-of-order processors, register renaming, Multithreading, Multiprocessors.
8 Hours

TEXT BOOKS:		
1	Sarah L Harris David Money Harris	Digital Design and Computer Architecture RISC-V Edition, Morgan Kaufmann Publishers, 2022.
2	David Patterson, Andrew Waterman	RISC-V Reader: An Open Architecture Atlas, Strawberry Canyon, 1st Edition, 2017

REFERENCE BOOKS:		
1	David A. Patterson John L. Hennessy	Computer Organization and Design The Hardware/Software Interface RISC-V Edition, Morgan Kaufmann Publishers, 2020
2	Edson Borin	Introduction to Assembly programming with RISC-V, 1st Edition, 2024, ISBN:978-65-00-15811-3
3	Anthony J Dos Reis	RISC-V Assembly Language, 2019 ISBN-13 : 978-1088462003

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Develop** Assembly level programs for basic arithmetic and logical operations using RISC-V processor.
CO2	**Interpret** Assembly level instructions of RISC-V in to its Machine level code.
CO3	**Design** RISC-V Microarchitectures.
CO4	**Develop** HDL for different elements of RISC-V design.
CO5	**Design** pipelined RISC-V processor architecture.

Mixed Signal Circuit Design

Contact Hours/ Week:	3+0+0 (L+T+P)	Credits:	3.0
Total Lecture Hours:	42	CIE Marks:	50
Total Tutorial Hours:	0	SEE Marks:	50
Total Practical Hours:	0	Course Code:	
Course Type:	PEC	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	Enable students to understand the various integrated based filters, data converters, integrated circuit of oscillators and PLLs in IC design.

UNIT I
Submicron CMOS Circuit Design: Submicron CMOS: Overview and Models, CMOS process flow, Capacitors and Resistors. Digital circuit design: The MOSFET Switch, Delay Elements, An Adder. Analog Circuit Design: Biasing, Op-Amp Design, Circuit Noise.
8 Hours

UNIT II
Integrator Based CMOS Filters: Integrator Building Blocks- low pass filter, Active RC integrators, MOSFET-C Integrators, gm-C integrators, discrete time integrators. Filtering Topologies: The Bilinear transfer function, The Biquadratic transfer function, Filters using Noise shaping.
8 Hours

UNIT III
Data Converter Modeling and SNR: Sampling and Aliasing: Modeling approach, Impulse sampling, sample and Hold, Quantization noise. Data converter SNR: An overview, Clock Jitter, Improving SNR using Averaging, Decimating filter for ADCs, Interpolating filter for DACs, Band pass and High pass sinc filters - Using feedback to improve SNR.
9 Hours

UNIT IV
Sampling Circuits and Switched Capacitor Circuits: Basic Sampling Circuits: NMOS switch , PMOS switch, Transmission gate switch, Distortion due to switches, Speed and precision considerations, Charge injection, Charge injection cancellation, Bottom-plate sampling, Gate-bootstrapped switch Switched Capacitor Circuits: Sampling switches, Switched capacitor amplifiers and Parasitic-insensitive SC amplifiers
9 Hours

UNIT V
Comparator Design: Preamplification, Decision circuit, Output buffer, Comparator DC performance, Transient response, Clocked comparators **Bandgap References and Biasing Circuits:** General considerations, Supply-independent biasing, PTAT current generation and Constant-Gm biasing.
8 Hours

Text Books:		
1	R.Jacob Baker	CMOS Mixed Signal Circuit Design, 2nd Edition, Wiley India, IEEE Press, reprint 2008.
2	R.Jacob Baker	CMOS Circuit Design, Layout and Simulation, 4th Edition, Wiley India, IEEE Press, 2019.
3	Behzad Razavi	Design of Analog CMOS Integrated Circuits, 2nd Edition, McGraw Hill, 2017.

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Describe** the concepts for mixed signal MOS circuit.
CO2	**Analyze** the characteristics of IC based CMOS filters.
CO3	**Analyze** the signal to noise ratio and modeling of mixed signals
CO4	**Apply** sampling and switched-capacitor techniques in analog circuit design.
CO5	**Design** comparators, voltage reference, and biasing circuits for mixed-signal applications.

PROFESSIONAL ELECTIVE – IV

CMOS RF Circuit Design

Contact Hours/ Week:	3+0+0 (L+T+P)	Credits:	3.0
Total Lecture Hours:	42	CIE Marks:	50
Total Tutorial Hours:	0	SEE Marks:	50
Total Practical Hours:	0	Course Code:	
Course Type:	PEC	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	To impart the knowledge on designing CMOS RF Circuit.

UNIT I
Introduction to RF Design and Wireless Technology: Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Intersymbol interference, random processes and noise, Sensitivity and dynamic range, conversion of gains and distortion, characteristics of passive IC components, resistor, capacitor and inductor.
9 Hours

UNIT II
RF Modulation: Analog Modulation: Amplitude Modulation, Phase and Frequency Modulation, Digital modulation: Basic concepts, Binary Modulation, Quadrature Modulation. Power efficiency of modulation schemes, Coherent and Non-coherent detectors. Mobile RF communication, basics of multiple access techniques and wireless standards.
8 Hours

UNIT III
Transceiver Architectures: Receiver Architecture: Heterodyne, Homo dyne, Image Reject Receiver and Transmitter Architecture. **Distributed Systems:** Transmission lines, reflection coefficient, the wave equation, examples, Lossy transmission lines, Smith charts – plotting gamma. **High Frequency Amplifier Design:** Bandwidth estimation using open-circuit time constants, Bandwidth estimation using short-circuit time constants, Rise time, delay and bandwidth, Zeros to enhance band width, Shunt-series amplifiers, tuned amplifiers, and Cascaded amplifiers.
8 Hours

UNIT IV
Low noise Amplifier design: CS stage: Inductive load, Resistive Feedback, Inductive degeneration. Variants of CS LNA, Noise – Cancelling LNAs, Differential LNAs. Non linearity Calculations in LNAs. **Mixers:** Mixer Nose Figures, Port – Port Feed through, Single –balanced and double balanced Mixers, Introduction to Passive and Active Mixers.
8 Hours

UNIT V
Oscillators: General Principles: Feedback view, One-Port view, Cross-Coupled Oscillator, Three – Point Oscillators. Voltage Controller Oscillators (VCO): Tuning Limitations, Effect of varactor Q, VCOs with wide tuning Range. Effect of Phase Noise, Low noise VCOs. **Phase Locked Loop (PLL):** Type – I PLLs: VCO phase Alignment, Dynamics of Type – 1 PLLs, Frequency Multiplication, drawbacks of Type – 1 PLL. Type-II PLLs: Phase/Frequency Detectors, Charge Pumps, Charge-Pump PLLs, Transient Response. **Integer N Frequency Synthesizer:** Basic integer N Frequency Synthesizer, Setting behavior, Spur reduction technique.
9 Hours

Text Books:		
1	B. Razavi	RF Microelectronics, PHI, 2nd Edition, 2011
2	R. Jacob Baker, H.W. Li, D.E. Boyce	CMOS Circuit Design, layout and Simulation, PHI, 2nd Edition, 2004.
Reference Books:		
1	Thomas H. Lee	Design of CMOS RF Integrated Circuits, Cambridge University press, 2nd Edition, 2003.
2	Y.P. Tsividis	Mixed Analog and Digital Devices and Technology, TMH, 2010

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Analyze** the performance parameters to be considered for the design of RF circuits
CO2	**Select** the suitable modulation technique and RF communication concepts for RF circuit design.
CO3	**Analyze** various Transceiver architecture and bandwidth estimation techniques.
CO4	**Analyze** low-noise amplifiers and mixers by evaluating gain, noise, linearity, and performance trade-offs in RF receiver front-end circuits.
CO5	**Design** oscillators, VCOs, PLLs, and frequency synthesizers by evaluating tuning range, phase noise, transient response, and frequency generation techniques in RF systems.

Design of CMOS Phase Locked Loops

Contact Hours/ Week:	3+0+0 (L+T+P)	Credits:	3.0
Total Lecture Hours:	42	CIE Marks:	50
Total Tutorial Hours:	0	SEE Marks:	50
Total Practical Hours:	0	Course Code:	
Course Type:	PEC	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	To impart the knowledge of designing phase locked loops, Delay locked loops.

UNIT I
Introduction: Introduction to Phase locked loops (PLLs), Basic operation of PLL and DLL architectures. Steady state analysis of basic PLL architectures.
9 Hours

UNIT II
Designing PFD and Charge pump: Phase detectors, Phase frequency detectors, Charge pump, Loop filters, Introduction to Charge pump based PLLs, Design methodology of charge pump based PLLs.
8 Hours

UNIT III
Oscillators: Basic principles, Cross coupled oscillators, Voltage controlled oscillators, VCOs with wide tuning range, Basic concepts, of phase noise. Inverter based Ring oscillators, Basic differential ring oscillators.
8 Hours

UNIT IV
Frequency synthesis: Introduction to frequency synthesis, Basic Integer N – Synthesizer, Divider design: Pulse swallow divider, Dual modulus divider, Divider logic styles. Fractional N – Synthesizer: Basic concepts, Fractional divider using Delta sigma modulation technique.
8 Hours

UNIT V
Digital PLL (DPLL): Basic architecture of DPLL, Basic operation of Time to Digital conversion (TDC), Vernier TDC, Digitally controlled oscillator. Basics of Digital filters. **Clock and Data recovery circuits:** Basic idea of clock and data recovery circuits, Bang-Bang Phase detector, Alexander phase detector, Hogge Phase detector.
9 Hours

TEXT BOOKS:		
1	Behzad Razavi	Design of CMOS Phase locked loops, from circuit level to Architecture level, Cambridge university press, 2020.
2	Behzad Razavi	RF microelectronics, 2nd Edition Pearson education 2012

REFERENCE BOOKS:		
1	F. Gardner	Phaselock Techniques, John Wiley & Sons, 2005.
2	R. Best	Phase-Locked Loops: Design, Simulation, and Applications, McGraw Hill, 2007.

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Analyze** PLL architecture.
CO2	**Design** PFDs and Charge pumps
CO3	**Design** VCOs and Ring oscillators.
CO4	**Design** dual modulus, integer -N and fractional dividers, Charge pump based Integer N and fractional PLLs.
CO5	**Analyze** digital phase-locked loops (DPLLs) and clock/data recovery circuits using TDCs, digital filters, DCOs, and phase detection techniques for high-speed communication systems.

Hardware Security Systems

Contact Hours/ Week:	3+0+0 (L+T+P)	Credits:	3.0
Total Lecture Hours:	42	CIE Marks:	50
Total Tutorial Hours:	0	SEE Marks:	50
Total Practical Hours:	0	Course Code:	
Course Type:	PEC	Exam Hours:	3

Course objectives: This course will enable students to:	
1.	To impart the knowledge on Hardware security and its implementation.

UNIT I
Introduction: Introduction to modern cryptography and hardware security, Symmetric Key and Assymetric key cryptography, Historical ciphers, Perfect security and its limitations. Pseudo random number generators (PRGs), Secure and practical instantiation of PRGs.
8 Hours

UNIT II
Cryptanalysis: Introduction to Crypto analysis, Block ciphers, Inner structure of block ciphers, Advanced encryption standard (AES), Key scheduling in AES, Quantum safe cryptography, Field isomorphisms. **Hardware design of AES:** Algorithm and architectural optimizations for AES Design, Circuit for the AES s-box, Implementation of the mixcolumns transformation. Compact AES s-box, Compact AES s-box on a normal basis
9 Hours

UNIT III
Finite Field Arithmetic: Finite Field architectures, Hardware design and architecture for Finite field inverse. **Elliptic curve cryptography (ECC):** Introduction ECC, Elliptic curve cryptoprocessor (ECCP). Point arithmetic on the ECCP, The Finite state machine of ECCP, Pipelining strategies for the scalar multiplier.
9 Hours

UNIT IV
Side Channel Analysis: Introduction to side channel analysis, Types of side channel attacks, Difference between Side channel analysis and Conventional Cryptanalysis **Power Analysis:** Introduction to power analysis, power attacks, differential power attacks, Power counter measures.
8 Hours

UNIT V
Fault Analysis: Fault analysis of Crypto systems, Improved differential fault analysis (DFA) of AES, Multibyte and key scheduling based fault analysis of AES, Redundancy based fault intensity. **Micro architectural attacks:** Cache timing attacks on block ciphers, Branch prediction attacks, Row hammer attacks. **Public key cryptosystem:** RSA public key cryptosystem, Hybrid public key cryptosystem.
8 Hours

TEXT BOOKS:		
1	Debdeep Mukhopadhyay, Rajat Subhra chakraborty	Hardware Security, Design, threats and safeguards, CRC press, 2015
2	Bhunia, Swarup and TEhranipoor	Hardware Security: A hands-on learning Approach. United Kingdom, Elsevier Science, 2026.

REFERENCE BOOK:		
1	Roger R. Dube	Hardware-Based Computer Security Techniques to Defeat Hackers - From Biometrics to Quantum Cryptography, John Wiley & Sons Inc; 1st edition, 2008.

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Apply** cryptographic principles to realize secure hardware system.
CO2	**Analyze** block cipher structures to optimize hardware architectures
CO3	**Develop** hardware architectures for finite field arithmetic and elliptic curve cryptoprocessors (ECCP).
CO4	**Analyze** side-channel and power analysis attack vectors to determine the vulnerabilities of cryptographic hardware.
CO5	**Develop** redundancy-based countermeasures to mitigate differential fault analysis (DFA) in cryptographic systems.

VLSI Design Lab

Contact Hours/ Week:	0+0+2 (L+T+P)	Credits:	1
Total Lecture Hours:	0	CIE Marks:	50
Total Tutorial Hours:	0	SEE Marks:	50
Total Practical Hours:	28	Course Code:	
Course Type:	PCCL	Exam Hours:	3

Course objectives:	
This course will enable students to:	
1.	Analyse, Design and simulate digital and analog MOSFET circuits for various applications.

List of Experiments:	
1.	Design a given logical operation using CMOS design style. a. Draw the schematic and verify the design parameters with the help of i. Transient Analysis to verify the truth table b. Draw the Layout and verify the DRC. c. Extract RC and back annotate the same and verify the Design
2.	Design a CMOS full adder for given specifications. a. Draw the schematic and verify the design parameters with the help of i. Transient Analysis to verify the truth table b. Draw the Layout and verify the DRC. c. Extract RC and back annotate the same and verify the Design
3.	Design a Common Source amplifier with resistive load for given specifications. a. Draw the schematic and verify the design parameters with the help of i. DC Analysis (Calculate the theoretical value for Av) ii. Transient Analysis (Verify theoretical value of Av with its Practical value). b. Draw the Layout and verify the DRC, LVS c. Extract RC and back annotate the same and verify the Design
4.	Design a Common Source amplifier with Active load using Current mirror for given specifications. Complete the design flow mentioned below: a. Draw the schematic and verify the design parameters with the help of i. DC Analysis (Calculate the theoretical value for Av) ii. Transient Analysis (Verify theoretical value of Av with its Practical value). b. Draw the Layout and verify the DRC, LVS c. Extract RC and back annotate the same and verify the Design

5.	Design a Common drain amplifier with Active load for given specifications. Complete the design flow mentioned below: a. Draw the schematic and verify the design parameters with the help of i. DC Analysis (Calculate the theoretical value for Av) ii. Transient Analysis (Verify theoretical value of Av with its Practical value). b. Draw the Layout and verify the DRC, LVS Extract RC and back annotate the same and verify the Design
6.	Design a Differential Amplifier with Active load using Current mirror for given specifications. Complete the design flow mentioned below: a. Draw the schematic and verify the design parameters with the help of i. DC Analysis (Calculate the theoretical value for Av) ii. Transient Analysis (Verify theoretical value of Av with its Practical value). b. Draw the Layout and verify the DRC, LVS. Extract RC and back annotate the same and verify the Design.
7.	Design a Operational Amplifier with Active load using Current mirror for given specifications. Complete the design flow mentioned below: a. Draw the schematic and verify the design parameters with the help of i. DC Analysis ii. Transient Analysis b. Draw the Layout and verify the DRC, LVS Extract RC and back annotate the same and verify the design
8.	Design a 4 bit binary weighted DAC / 4-bit R-2R Ladder DAC for given specifications. Complete the design flow mentioned below: a. Draw the schematic and verify the design parameters with the help of i. DC Analysis ii. Transient Analysis b. Draw the Layout and verify the DRC, LVS Extract RC and back annotate the same and verify the design

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Design** analog circuits and simulate using EDA tool and prepare the report.
CO2	**Design** digital circuits and simulate using EDA tool and prepare the report.

Minor Project

Contact Hours/ Week:	0+0+4 (L+T+P)	Credits:	2
Total Lecture Hours:	0	CIE Marks:	50
Total Tutorial Hours:	0	SEE Marks:	50
Total Practical Hours:	60	Course Code:	
Course Type:	Project	Exam Hours:	3

Course objective:

Course objectives: This course will enable students to:	
1.	The objective of this course is to provide students with an opportunity to apply the theoretical concepts and practical skills acquired in VLSI Design and Embedded Systems to solve real-world engineering problems.

Course Outcomes: Upon completion of this course the student will be able to:	
CO1	**Conduct** a systematic literature review in VLSI Design and Embedded Systems to identify research gaps and define a well-structured problem statement with appropriate design specifications. (PO7).
CO2	**Apply** advanced concepts of VLSI and Embedded Systems using modern EDA tools to design and implement a functional engineering solution. (PO5)
CO3	**Design, implement, test, and evaluate** VLSI circuits or embedded systems to analyze and validate system performance and functionality. (PO3, PO4)
CO4	**Prepare** well-structured project report, presentations, and communicate project outcomes effectively.(PO2)
CO5	**Demonstrate** effective **teamwork**, **project management** skills, and ethical practices in executing engineering projects and professional activities. (PO1, PO6)