

**Dr. Rakesh M B**

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Department of Electronics & Telecommunication Engg.,  
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**Education**

Sl. No.	Degree	Year	Institute	Specialization
1	PhD	2026	Indian Institute of Technology, Hyderabad.	Microelectronics and VLSI
2	M.Tech	2014	J.S.S.Academy of Technical Education, Bangalore.	VLSI Design and Embedded Systems
3	B.E.	2008	R.V. College of Engineering, Bangalore.	Electronics and Communication

**Professional Experience**

Sl. No.	Date (from-to)	Designation	Organization
1	July 2015 – till date	Assistant Professor	Siddaganga Institute of Technology (SIT), Tumkur.
2	July 2014 – May 2015	Assistant Professor	DYPSOEA, Pune.
3	October 2008 – March 2009	Assistant System Engineer	TCS, Mumbai.

## Courses Taught

1. Introduction to AI and Applications.
2. Digital Electronic Circuits Design and Verilog.
3. Processor Controller and Architecture.
4. Embedded Systems.
5. Electronic Measurements & Instrumentation.
6. Switching Logic and Finite Automata Theory.
7. Real Time Systems.
8. Linear, Mixed Signals and RF IC's.
9. Analog MOS circuits Design.

## Research Areas

- Machine Learning in VLSI EDA.
- Low Power VLSI Design.

## Publications

### Journals:

1. **Rakesh M B**, Anant Terkar, Pabitra Das and Amit Acharyya, "GARNETT: Graph-based Fast yet Accurate Post-Placement Toggle Rate Prediction Model from RTL without Technology-dependent Logic Synthesis and Placement", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, February 2026.
2. **Rakesh M B**, Pabitra Das, Sai Pranav K R and Amit Acharyya, "GRIPT: Graph Attention-assisted Inductive Methodology for Fast and Accurate Average Power Estimation from RTL Simulation skipping Gate-level Simulation", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 44, no. 11, pp. 4209-4221, Nov. 2025.
3. **Rakesh M B**, Pabitra Das, Sai Pranav K R and Amit Acharyya, "Inductive GNN-based Methodology for Accurate and Fast Average Power Estimation of Synthesized ASIC Designs from RTL Simulation bypassing Gate-level Simulation", in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 72, no. 6, pp. 2818-2831, June 2025.
4. **Vatti Chandrasekhara Srinivas, M. B. Rakesh, P. Ravi Teja Reddy, and Amit Acharyya**. "A Hierarchical Fault-Tolerant and Cost Effective Framework for RRAM Based Neural Computing Systems", in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 3, pp. 684-688, March 2022.

### Conference Proceedings:

1. Arpit Jain, Pabitra Das, **Rakesh M B** and Amit Acharyya, "ANN Based Accurate and Fast Post-Route QoR Data Prediction Methodology from Pre-Clock Tree Synthesis by Skipping CTS and Routing", **2024 IEEE International Symposium on Circuits and Systems (ISCAS), Singapore**, July 2024, pp. 1-5.
2. **Rakesh M B**, Pabitra Das and Amit Acharyya , "GRASPE: Accurate Post-Synthesis Power Estimation from RTL Using Graph Representation Learning", **2023 IEEE International Symposium on Circuits and Systems (ISCAS), Monterey, CA, USA**, July 2023, pp. 1-5.
3. **Rakesh M B**, Pabitra Das, Sai Pranav K R and Amit Acharyya , "GRILAPE: Graph Representation Inductive Learning-based Average Power Estimation for Frontend ASIC RTL Designs", **2023 36th International Conference on VLSI Design and 2023 22nd International Conference on Embedded Systems (VLSID)**, Hyderabad, India, May 2023, pp. 1-6.
4. **Rakesh M B**, Sai Pranav K R, Pabitra Das, and Amit Acharyya , "GLAAPE: Graph Learning Assisted Average Power Estimation for Gate-level Combinational Designs", **2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Glasgow, United Kingdom**, December 2022, pp. 1-4.
5. **Rakesh, M. B.** "Performance comparison of 8 bit & 32 bit logarithmic barrel shifter using Fredkin & SCRL gates." *2017 International Conference on Circuits, Controls, and Communications (CCUBE)*, Bangalore, India, June 2018, pp. 7-10.
6. **Rakesh M B**, "Implementation of 32 bit Logarithmic Barrel Shifter using SCRL gate.", in National Conference on VLSI Signal and Image processing,NCVSIP-14,Bangalore, August 22-23,2014
7. **Rakesh M B**, "Low Power Reversible Logarithmic Barrel Shifter for MAC application.", in National Conference on Recent Advances in Communication Networks, NCRAN'14, March 21- 22,2014.

### Patents:

1. **Rakesh M B**, Pabitra Das and Amit Acharyya "Graph Representation Learning-based Average Power Estimation of Synthesized ASIC RTL Designs", Indian Institute of Technology, Hyderabad. (**Indian Patent 556481**, Application No. 202341047558, Publication Date: 01/09/2023, **Granted Date: December 18, 2024**).
2. **Rakesh M B**, Pabitra Das and Amit Acharyya "Machine Learning Methodology for Predicting Toggle Rates in Application Specific Integrated Circuit", Indian Institute of Technology, Hyderabad. [Application No. 202541078951, **Publication Date: 29/08/2025**].