

CURRICULUM VITAE

C/O B P Raju
Brahmendra Dhama
Devanoor Road,
Opp to chennappana palya
Upparalli, TUMKUR
MobileNo: 9901188715

VINAYA S J

Email: vinay.jjachar@gmail.com

OBJECTIVE

Seeking a position to utilize my skills and abilities in an Organization that offers professional growth while being resourceful, innovative and flexible.

Work Experience

1. Internship at Innovative logic India pvt.ltd, Bangalore

Title: Design of Modules for verification of WUSB Device Using System Verilog

Team Size: 1

Project Duration: 9 months

Description: The wireless USB defines a short-range wireless replacement for the present wired USB interface, with a data rate of 480 Mbps at 3 meters. The architecture of Wireless USB is a classic hub and spoke, where the host (user's PC) communicates directly with up to 127 USB devices. There is only one HOST in USB system. The Host has to initiate all data transfers.

In order to check the functionalities of a WUSB Device IP, we need to have verification model. A verification environment has to be designed to verify the different functionalities of our WUSB device IP using System Verilog.

The main focus of this project is to setup a verification environment using system verilog to verify functionality of wireless USB device (IP). In this regard, this project deals with the implementation of modules in a verification environment using System Verilog.

Professional Experience:

Total Teaching Experience: 15 Years

Assistant Professor, SIT Tumakuru (On deputation for Ph.D.)

Project Trainee, Innovative Logic India Pvt. Ltd., Bangalore

Research Focus

SOI Junctionless FinFET Devices, Short Channel Effects, BSIM-CMG Modeling,
Neuromorphic Circuits

Educational Details:

<i>Education</i>					
Qualifying Examination	College	University	Year of passing	Class	Percentage
M.Tech VLSI Design & Embedded Systems	Dayanand Sagar College of Engineering Bangalore	VTU Visvesvarya Technological University	2008	First class with distinction	Aggregate of all semesters 72%
B.E. Electronics & Communication	Siddaganga Institute of Technology Tumkur, Karnataka.	VTU Visvesvarya Technological University	2003	First class	Aggregate of all semesters 62%
P.U.C.	D.V.S(IND)PU College, Shimoga Karnataka.	Karnataka Pre University Board	1999	First class	86%
S.S.L.C.	B.L.R PU College, Sirigere, Karnataka.	KSEEB	1997	First class	86%

Technical Skills:

- HDL Verilog, System Verilog
- Simulation Tool Modelsim
- Synthesis Tool Design compiler
- STA-tool PrimeTime

BE Final Semester Project

Title: E-HOST and monitoring system using - 8051 microcontroller.

Team Size: 3

Project Duration: 3 months

Description:

E-host as the name implies is electronic host which can be used either in the house or in the office to provide master to interact with visitors in a pleasant and smart way. In *E-host* the visitor will have a *smart card* in which his details regarding his name and other information will be stored .when he puts the card he will be identified and he has to type the code, if the code is correct then it will display the message intended for him.In addition to all these smoke detector, panic switches and reed switches to indicate emergency situations like intruder into house or office and to control external devices like motors, exhaust fans and alarm.

Personal skills:

- Good verbal and written English, interests in innovating new ideas, Willingness to learn, team facilitator, good leadership quality, creative thinking.

Personal Details:

Father's Name : Jayannachar
Date of Birth : 14th DEC 1981
Nationality : Indian
Marital status : Single
Languages Known : Kannada, English, Hindi.

Other Achievements:

- Participated in a two day HRD Programme “Feel Employable” at S.I.T TUMKUR
- Won “BEST PROJECT “award for B E Final year project at SIT, TUMKUR in 2003.
- Attended Faculty development programme at AIT, Bangalore Organized by VTU IN 2006
- Attended *MISSION-10X* workshop organized by **WIPRO** in 2009.
- Involved in *campus connect* programmes as a trainer by **Infosys**.

Publications:

[1].S. J. Vinaya and K. S. Nikhil, “Impact of gate oxide thickness variation on the on-state safe operating area and FoM of SOI-Junctionless FinFET considering the self-heating effects,” in Proc. 2024 11th Int. Conf. on Advances in Computing and Communications (ICACC), IEEE, 2024,pp. 1–5.

[2]. V. S. J., R. Rao, and K. S. Nikhil, “Investigation of the impact of gate oxide thickness variation of junction-less FinFET using BSIM-CMG model for LIF neuron and STDP circuit application,”Phys. Scr., accepted for publication, 2025. [IOP Publishing]

[3]. V. S. J., R. Rao, and K. S. Nikhil, “Modeling the dependence of short-channel effects on the silicon thickness and gate oxide thickness of FinFETs,” (to be submitted to IOP *journal: Modelling and Simulation in Materials Science and Engineering*)

Date :

Place: Tumkur

VINAYA S.J

