SIDDAGANGA INSTITUTE OF TECHNOLOGY, TUMAKURU

LECTURE PLAN FOR THE ACADEMIC YEAR 2023 – 2024

Teacher	Dr. RUDRAMURTHY M S	**Dept.**	Information Science & Engineering
Class	III Semester, E Section	**Course**	**Integrated Course:** S3ISI01: Digital Circuits & Computer Organization
Contact Hrs/Week	3L+0T (Credits: 4.0)		CIE Marks: 50 SEE Marks: 50

Course objectives: This course will enable students to:	
1.	Learn the different techniques of simplification of Boolean expressions and design of combinational circuits.
2.	Design of counters and registers for the real time applications.
3.	Understand the fundamental concepts of computer organization and gain insight into the addressing modes and execution of an instruction in a single bus CPU.
4.	Apply the different computer arithmetic techniques to solve the problems.

SL. No.	DATE	TOPIC	REMARKS
		UNIT – I	
1	07-11-2023	**Introduction to Digital System:** Boolean Algebra and Boolean Functions,	
2	09-11-2023	min-term and max-term notations. Simplification of Boolean expressions using Boolean laws and Rules,	
3	10-11-2023	Simplification of Boolean expressions using Boolean laws and Rules,	
4	16-11-2023	Simplification of Boolean expressions using Karnaugh map techniques.	
5	17-11-2023	Simplification of Boolean expressions using Karnaugh map techniques	
6	21-11-2023	Simplification of Boolean expressions using Karnaugh map techniques	
7	23-11-2023	Design of combinational Logic Circuits:	
8	24-11-2023	Design of Decoders,	
9	28-11-2023	Multiplexers, DeMultiplexers.	Assignment 1
		UNIT-II	
10	01-12-2023	**Sequential Logic Circuits:** **Flip Flops:** Introduction to Flip-Flops,	
11	05-12-2023	Types of Flip-Flops: RS FF, SR FF,	
12	07-12-2023	JK FF and M/S JK FF.	
13	08-12-2023	**Counters:** Definition of Counter, Types of Counters, Design of Asynchronous Counters.	
14	12-12-2023	**Registers:** Basic Register, Shift-Register, Types of Shift Registers,	
15	14-12-2023	Unidirectional and Bidirectional Shift Register,	
16	15-12-2023	Johnson counter and Ring Counters.	Assignment 2

		UNIT-III	
17	19-12-2023	**Basic Structure of Computer:** Functional Units,	
18	21-12-2023	Basic Operational Concepts, Bus Structures,	
19	22-12-2023	Performance - Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement.	
20	26-12-2023	Machine Instructions and Programs: Numbers, Arithmetic Operations and	
21	28-12-2023	Characters - Number Representation,	
22	29-12-2023	Addition of Positive Numbers,	
23	02-01-2024	Addition and Subtraction of Signed Numbers,	
24	04-01-2024	Overflow in Integer Arithmetic,	
25	05-01-2024	Characters, Memory Location and Addresses - Byte Addressability	Assignment 3
		UNIT-IV	
26	09-01-2024	**Addressing modes**-Implementation of Variables and Constants,	
27	11-01-2024	Indirection and Pointers, Indexing and Arrays, Relative Addressing, Additional Modes.	
28	12-01-2024	**Basic Processing Unit:** Execution of a Complete Instruction	
29	16-01-2024	Branch Instructions, Multiple Bus Organization,	
30	18-01-2024	Design of Asynchronous Up and Down Counters.	
31	19-01-2024	Hard wired Control - A Complete Processor,	
32	23-01-2024	Micro programmed Control -Microinstructions.	Assignment 4
		UNIT-V	
33	25-01-2024	**Arithmetic**: Addition and Subtraction of Signed Numbers - Addition/Subtraction Logic Unit,	
34	30-01-2024	Multiplication of Positive Numbers,	
35	01-02-2024	Signed Operand Multiplication - Booth Algorithm,	
36	02-02-2024	Fast Multiplication - Bit-Pair Recoding of Multipliers,	Assignment 5
37	06-02-2024	Carry-Save Addition of Summands, Integer Division,	
38	09-02-2024	Floating-point Numbers and Operations - IEEE Standard for Floating-Point Numbers,	
39	14-02-2024	Arithmetic Operations on Floating-Point Numbers - Addition and Subtraction Operations	
40	15-02-2024	Arithmetic Operations on Floating-Point Numbers - Addition and Subtraction Operations	
41	17-02-2024	Arithmetic Operations on Floating-Point Numbers - Addition and Subtraction Operations	

TEXT BOOKS:

1.	Thomas L Floyd, Digital Fundamentals	Digital Fundamentals, Pearson Publications. Ed.11, 2020.
2.	Carl Hamacher, Zvonko Vranesic, SafwatZaky	Computer Organization, Tata McGraw Hill, ED.5, 2017

REFERENCE BOOKS:

1.	Donald P Leach, Albert Paul Malvino and Goutam Saha	Digital Principles and Applications, Tata McGraw – Hill, Ed.8, 2014
2.	Ronald J Tocci, Neil S Widmer, Gegory L. Moss.	Digital Systems-Principles and Applications, Pearson Education, Ed.12. 2016.

LABORATORY PROGRAMS LIST:

Sl.No	Dates	Experiment
1	06-11-2023, 08-11-2023 and 10-11-2023	Introduction to Electronics: Truth Table Verification of Basic Logic Gates.
2	13-11-2023, 15-11-2023 and 17-11-2023	Design and implementation of Half-adder and Full adder using minimum number of NAND gates only.
3	20-11-2023, 22-11-2023and 24-11-2023	Design and implement a 3-variable SOP expression using a dual 4:1 MUX IC74LS153.
4	27-11-2023, 29-11-2023and 01-12-2023	Design and implement the Full adder and Full subtractor using decoder and other logic gates.
5	04-12-2023, 06-12-2023 and 08-12-2023	Implement the following using 4-bit shift register IC 74LS95. a) Right Shift b) SISO c) PIPO d) PISO e) SIPO f) Left Shift g) Ring Counter h) Johnson Counter.
6	11-12-2023, 13-12-2023and 15-12-2023	**Test 1**
7	18-12-2023, 20-12-2023and 22-12-2023	Design a sequence generator to generate the given sequence using shift Register IC and other gates.
8	27-12-2023, 29-12-2023and 01-01-2024	Design and implement 3-stage Asynchronous (mod-8) counter using MS J-K flip flops IC7476.
9	03-01-2024, 05-01-2024 and 12-01-2024	Implement UP-Down pre-settable counter using IC 74LS190 for the given mod N.
10	17-01-2024, 19-01-2024 and 22-01-2024	Implement asynchronous mod-8 counter using decade counter IC74LS90 and decoder IC7447 to display values from 0 to 9 using 7-segment display.
11	24-01-2024, 29-01-2024 and 31-01-2024	Design and implementation of Three bit Synchronous Counter.
12	02-02-2024, 05-02-2024 and 07-02-2024, 09-02-2024, 14-02-2024, 16-02-2024	**Test 2 and Repetition classes**

Course Outcomes:

After the completion of this course, students will be able to:

CO1: **Design** combinational logic circuits for the required applications
CO2: **Design** sequential logic circuits such as counters and registers for the specific needs.
CO3: **Analyze** the performance of a basic computer system
CO4: **Design** control sequence for the given instruction on different CPU bus structures.
CO5: **Apply** appropriate technique to solve arithmetic related problems in computer

Mapping of Course Outcomes (COs) to Program Outcomes (POs) & Program Specific Outcomes (PSOs)

		POs												PSOs		
		1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
COs	CO1	2	2												2	
	CO2	2	2	2											2	
	CO3	2	2	1											2	
	CO4	2	2	1											2	
	CO5	2	1	1											2	
	AVG	2	2	2											2	

Assessment Tools	COs				
Direct AT	**CO1**	**CO2**	**CO3**	**CO4**	**CO5**
CIE (Individual)	√	√	√	√	√
SEE (Individual)	√	√	√	√	√
Assignments (Individual/Group)	√	√	√	√	√
Micro Projects (Group)	-	-	-	-	-
Topic seminar (Individual)	-	-	-	-	-
Case studies (Individual/Group)	-	-	-	-	-
Online courses (Individual)	-	-	-	-	-
Indirect AT	**CO1**	**CO2**	**CO3**	**CO4**	**CO5**
Course end survey (Students)	√	√	√	√	√
Student profile (Faculty)	-	-	-	-	-

Course delivery methods, assessment tools and sample questions:

CO1	**Design** combinational logic circuits for the required applications
Delivery Methods	Chalk and talk, PPT
Assessment Tools	CIE, SEE, Assignment
Sample Questions	Q1.Design a 3-to-8 line Decoder and show how it can be used to realize a Full adder. (L3) Q2.Design a 8:1 Multiplexer and show how it can be used to realize a Full adder. (L3)

CO2	**Design** sequential logic circuits such as counters and registers for the specific needs.
Delivery Methods	Chalk and talk, PPT
Assessment Tools	CIE, SEE, Assignment
Sample Question	Q1.Show how a T-FF can be used as a frequency divider. (L3) Q2. Design a three bit asynchronous UP and Down Counter using only M/S JK Flip Flops. Also, draw its timing diagram which illustrates the operation of the counter. (L3)

CO3	**Analyze** the performance of a basic computer system.
Delivery Methods	Chalk and talk, PPT
Assessment Tools	CIE, SEE, Assignment
Sample Question	Q1.The effective value of S for a RISC machine is 1.2 and for CISC, it is 1.5 both machines have the same clock rate R. The time for execution on the CISC machine is to be less than that of RISC machine. For this to happen, what is the largest allowable value for N, the number of instructions executed on the CISC machine, expressed as a percentage of the N value for the RISC machine. (L3) Q2. Explain the different basic instruction types. Show how the operation R=(A*B)-(C/D) can be implemented using any two instruction types.(L3)

CO4	**Design** control sequence for the given instruction on different CPU bus structures.
Delivery Methods	Chalk and talk, PPT
Assessment Tools	CIE, SEE, Assignment
Sample Question	Q1. Distinguish between Hardwired Controller and Microprogrammed Controller.(L2) Q2. Write the control signal sequence required to execute the instruction MOVE R2, (R1) in a Single bus CPU Organization.(L3)

CO5	**Apply** appropriate technique to solve arithmetic related problems in computer.
Delivery Methods	**Chalk&Talk/PPT**
Assessment Tools	Quiz, Test and Assignment
Sample Questions	Q1. Explain briefly the working principle of a Booth multiplier with an example. Give the flow chart for the Booth multiplication.(L3) 2. Multiply 13 and -6 using Bit-Pair Recoding of Multiplier method. (L3)

05/11/23
Teacher

06/11/23
HOD

06/11/2023
Principal

PRINCIPAL
Siddaganga Institute of Technology
TUMKUR - 572 103.

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Teacher **HOD** **Principal**

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Course Outcomes:

After the completion of this course, students will be able to:

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COs	CO1	2	2												2	
	CO2	2	2	2											2	
	CO3	2	2	1											2	
	CO4	2	2	1											2	
	CO5	2	1	1											2	
	AVG	2	2	2											2	

Assessment Tools	COs				
Direct AT	**CO1**	**CO2**	**CO3**	**CO4**	**CO5**
CIE (Individual)	√	√	√	√	√
SEE (Individual)	√	√	√	√	√
Assignments (Individual/Group)	√	√	√	√	√
Micro Projects (Group)	-	-	-	-	-
Topic seminar (Individual)	-	-	-	-	-
Case studies (Individual/Group)	-	-	-	-	-
Online courses (Individual)	-	-	-	-	-
Indirect AT	**CO1**	**CO2**	**CO3**	**CO4**	**CO5**
Course end survey (Students)	√	√	√	√	√
Student profile (Faculty)	-	-	-	-	-

Course delivery methods, assessment tools and sample questions:

CO1	**Design** combinational logic circuits for the required applications
Delivery Methods	Chalk and talk, PPT
Assessment Tools	CIE, SEE, Assignment
Sample Questions	Q1.Design a 3-to-8 line Decoder and show how it can be used to realize a Full adder. (L3) Q2.Design a 8:1 Multiplexer and show how it can be used to realize a Full adder. (L3)

CO2	**Design** sequential logic circuits such as counters and registers for the specific needs.
Delivery Methods	Chalk and talk, PPT
Assessment Tools	CIE, SEE, Assignment
Sample Question	Q1.Show how a T-FF can be used as a frequency divider. (L3) Q2. Design a three bit asynchronous UP and Down Counter using only M/S JK Flip Flops. Also, draw its timing diagram which illustrates the operation of the counter. (L3)

CO3	**Analyze** the performance of a basic computer system.
Delivery Methods	Chalk and talk, PPT
Assessment Tools	CIE, SEE, Assignment
Sample Question	Q1.The effective value of S for a RISC machine is 1.2 and for CISC, it is 1.5 both machines have the same clock rate R. The time for execution on the CISC machine is to be less than that of RISC machine. For this to happen, what is the largest allowable value for N, the number of instructions executed on the CISC machine, expressed as a percentage of the N value for the RISC machine. (L3) Q2. Explain the different basic instruction types. Show how the operation R=(A*B)-(C/D) can be implemented using any two instruction types.(L3)

CO4	**Design** control sequence for the given instruction on different CPU bus structures.
Delivery Methods	Chalk and talk, PPT
Assessment Tools	CIE, SEE, Assignment
Sample Question	Q1. Distinguish between Hardwired Controller and Microprogrammed Controller.(L2) Q2. Write the control signal sequence required to execute the instruction MOVE R2, (R1) in a Single bus CPU Organization.(L3)

CO5	**Apply** appropriate technique to solve arithmetic related problems in computer.
Delivery Methods	**Chalk&Talk/PPT**
Assessment Tools	Quiz, Test and Assignment
Sample Questions	Q1. Explain briefly the working principle of a Booth multiplier with an example. Give the flow chart for the Booth multiplication.(L3) 2. Multiply 13 and -6 using Bit-Pair Recoding of Multiplier method. (L3)

M.I Nadaraju 05.11.23
Teacher

06/11/2023
HOD

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Principal

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