ACADEMIC YEAR: 2025-26

SIDDAGANGA INSTITUTE OF TECHNOLOGY,
TUMAKURU 572103, KARNATAKA, INDIA

DEPARTMENT OF ELECTRONICS AND INSTRUMENTATION ENGINEERING

SYLLABUS

FOR

PG Course in

VLSI Design and Embedded Systems

2025-26

Siddaganga Institute of Technology, Tumkur-572103
Department of Electronics & Instrumentation Engineering
Programme: M.Tech - VLSI Design and Embedded Systems

Vision of the Institute
To develop thoughtful and creative young minds in a learning environment of high academic ambience by synergizing spiritual values and technological competence.

Mission of the Institute

1. To continuously strive for the total development of students by educating them in state-of-the-art-technologies and managerial competencies providing best in class learning experience with emphasis on skills, values and learning outcomes and helping them imbibe professional ethics and societal commitment.
2. To create a research ambience that promotes interdisciplinary research catering to the needs of industry and society.
3. To collaborate with premier academic and research institutions and industries to strengthen multidisciplinary education, applied research, innovation, entrepreneurship and consulting ecosystems.

Quality Policy

Siddaganga Institute of Technology is Committed to:
1. Impart Quality Education by establishing effective learning - teaching - learning processes to produce competent engineers and managers with high professional ethics and societal responsibility.
2. Create congenial environment and provide state-of the-art infrastructure.
3. Continually improve the effectiveness of the Quality Management System.
4. Satisfy applicable requirements.

Vision of the Department

To become a premier Electronics and Instrumentation Engineering Department by imparting quality education in the fields of electronics, instrumentation and cutting edge technologies developing competence to meet industrial norms and to pursue research and innovation contributing to socioeconomic development.

Mission of the Department

1. Develop competent professionals by offering industry aligned curriculum in Electronics, Instrumentation and VLSI and embedded systems along with an exposure to cutting edge technologies by providing best in class learning, promoting interdisciplinary research and innovation catering to industrial and societal needs.
2. Encourage and prepare students for higher studies to promote lifelong learning.
3. Imbibe professional ethics and skills in students to provide engineering service to the society.
4. Collaborate with industries to inculcate industry readiness, creativity, managerial competence, experiential learning and entrepreneurship skills.

Program Educational Objectives (PEOs):

PEO1: To build their **career in the core industry, public sector or multinational corporations**, in the domain of VLSI Design and Embedded systems.
PEO2: To **e**ngage in lifelong learning, excel in **research pursuits** and entrepreneur in technologies related to VLSI and Embedded Systems to meet the global challenges.
PEO3: To consistently exhibit **professional** and **ethical values**, **communication skills**, **team work and leadership** quality in their profession for the benefit of the society.
Program Outcomes (POs):

PO1 (Team Work): An ability to independently carry out research/investigation and development work to solve practical problems.
PO2 (Communication): An ability to write and present a substantial technical report/document.
PO3 (Scholarship of Knowledge): Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
PO4 (Problem Solving): The student will be able to think and solve engineering problems, evaluate a wide range of potential solutions for those problems, and arrive at feasible/optimal solutions.
PO5 (Usage of Modern Tools): The student will be able to apply modern engineering tools, equipment, and techniques to model and predict complex engineering problems with an understanding of the limitations.
PO6 (Project Management): The student will demonstrate knowledge and understanding of engineering and management principles and apply the same to one's own work, as a member and leader in a team, to manage projects efficiently and economically.
PO7 (Life-long Learning): The student will be able to recognize the need for, and demonstrate the ability to engage in lifelong learning independently with a high level of enthusiasm and commitment to improve knowledge and competency continuously.

Programme Specific Outcomes (PSOs):

PSO1: Apply the technical knowledge to **analyse, design, and implement VLSI system** and apply advanced concept in the field of semiconductor and emerging technologies.

PSO2: Apply the knowledge of **embedded system and Programming Skills** to design electronic system for real time applications.

SIDDAGANGA INSTITUTE OF TECHNOLOGY, TUMAKURU-03

(An autonomous Institute under Visvesvaraya Technological University)

SCHEME OF TEACHING AND EXAMINATION

I SEMESTER M.Tech. VLSI Design and Embedded Systems

I SEMESTER

	Course Type BSC/PCC / IPCC /PCC(PB) /	Course Code	Course Title	Teaching Hours per Week			Examination				Credits
				Theory	Practical/ Seminar	Tutorial/ SDA	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	P	T/SDA					
1	IPCC	S1LVSI01	Digital System Design using Verilog HDL	3	2	0	03	50	50	100	4
2	PCC(PB)	S1LVS02	VLSI Design	3	0	0	03	50	50	100	3
3	PCC	S1LVS03	ARM Microcontroller and its Applications	3	0	0	03	50	50	100	3
4	PCC	S1LVS04	Analog IC Design	3	0	0	03	50	50	100	3
5	PEC	S1LVSE1x	Professional Elective - I	3	0	0	03	50	50	100	3
6	PEC	S1LVSE2x	Professional Elective - II	3	0	0	03	50	50	100	3
7	PCCL	S1LVSL1	Embedded Systems Lab	0	4	0	03	50	50	100	2
8	NCMC	S1PGRM	Research Methodology and IPR	VTU Online course MRMI19							
	Total			18	6	0	21	**350**	**350**	**700**	**21**

Note: **BSC**-Basic Science Courses, **PCC**: Professional core. **IPCC**-Integrated Professional Core Courses, **PCC(PB):** Professional Core Courses (Project Based), **PCCL**-Professional Core Course lab **, NCMC**- None Credit Mandatory Course, ,**L**-Lecture**, P**-Practical**, T/SDA**-Tutorial **/** Skill Development Activities (Hours are for Interaction between faculty and students) **MRMI19**- Research Methodology and IPR (**Online**) for the students who have **not studied** this course in the Undergraduate level. This course is not counted for vertical progression, Students have to qualify for the award of the master's degree.

M- Master program **xx** – **ME** for Mechanical Engineering Stream, **CV** for Civil Engineering Stream, **EE** – Electrical & Electronics Engineering Stream, **EC**-Electronics and Communication Engineering Stream, **CS**- Computer Science and Engineering **BA** - Business Administration **AR**- Architecture- etc.

BSC: Basic Science Courses: Courses like Mathematics/ Science are the prerequisite courses that the concerned engineering stream board of Studies will decide. **PCC: Professional Core Course:** Courses related to the stream of engineering, which will have both CIE and SEE components, students have to qualify in the course for the award of the degree. **Integrated Professional Core Course (IPCC)**: Refers to a Professional Theory Core Course Integrated with practicals of the same course. The IPCC's theory part shall be evaluated by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. **Project Based Learning Course (PCC(PB):** Project Based Learning course is a professional core Course only Students have to complete a project out of learning from the course and SEE will be viva voce on project work. **PCCL: Professional Core Course Laboratory:** Practical courses whose CIE will be evaluated by the class teacher and SEE will be evaluated by the two examiners.

Skill development activities: Under Skill development activities in a concerning course, the students should

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustomed to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in the modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s are to be involved either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities that will enhance their skills. The prepared report shall be evaluated for CIE marks.

MRMI19-Research Methodology and IPR- Non Credit Mandatory Course (NCMC) if students have not studied this course in their undergraduate program then he /she has to take this course at **http://online.vtu.ac.in** and to qualify for this course is compulsory before completion of the minimum duration of the program (Two years), however, this course will not be considered for vertical progression.

Professional Elective - I		**Professional Elective - II**	
Course Code	**Course Title**	**Course Code**	**Course Title**
S1LVSE11	ASIC Design	S1LVSE21	Data Structures
S1LVSE12	VLSI Design Automation	S1LVSE22	Low power VLSI Design
S1LVSE13	VLSI for Digital Signal Processing	S1LVSE23	VLSI Testing and Verification

Digital System Design Using Verilog HDL

Contact Hours/ Week	: 3+2+0 (L+P+T/SDA)	Credits :	4.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Practical Hours	: 28	SEE Marks :	50
Course Code	: S1LVSI01	Course Type:	IPCC

Course Objective: To study and design various digital circuits and systems using Verilog Hardware Description Language (HDL), synthesize and implement on Field Programmable Gate Arrays (FPGAs).

UNIT- I

Introduction to HDL based Digital Design: Design flow and Design styles for digital circuits, Verilog operators, Verilog Primitives, Gate level, Data flow and Behavioral modeling. Delay models, Control statements, Tasks and Functions.

09 Hrs

UNIT- II

Programmable Logic Devices: ROM, PAL, PLA, CPLD, FPGA, FPGA Architecture, FPGA-CLBs, switch Matrix and IOB, Configurable Logic Blocks (CLBs) in Xilinx FPGA –XC3000 and Xilinx Spartan-7, FPGA Design Flow.

FPGA architectures and its usage in embedded Systems: Zynq Ultrascale + MPSoC device architecture. Introduction to Ultrascale Architectecture, System block diagram, High speed serial IO, MIO and EMIO, Functional units and peripherals, Signals interfaces and pins, On chip memory, DMA controller, Reset system, PL peripherals, Vivado design flow, Logic design on Ultrascale + MPSoC FPGA on PL block. Programming and debugging using SDK.

08 Hrs

UNIT- III

Fixed and Floating point Arithmetic: Fixed point number system and floating point number system, Arithmetic operation on Fixed and Floating point numbers. Combinational circuit design using Verilog:

Ripple Carry adder, Comparators, Combinational Multiplier – Array Multiplier, Unsigned and Signed integer multiplication, Barrel shifter, Tri-State Combinational Circuits.

08 Hrs

UNIT- IV

Sequential Circuit Design using Verilog: Latches, Flip Flops, Shift registers, Counters/ Timers/ Clock Dividers using T Flip Flops, Clock Dividers using D Flip Flops, Synchronous sequential Circuit Design using D and JK Flip Flops.

Finite State Machines (FSM): Finite State Machines and controllers, State diagram, designing FSM using state graph, one-hot-state assignment, controller design. Traffic Light control system.

09 Hrs

UNIT- V

Designing Data path components and Memory units: Serial adder, multiplier using Shift and Add, Fixed point and, Binary Divider, Accumulator, Booth Multiplier, Multiply and Accumulate (MAC) unit, Floating point Multiplier. Memory Design – FIFO, Stack, Circular Buffer.

08 Hrs

Reference Books:

1	Frank Vahid	Digital Design with RTL Design, VHDL, and Verilog 2nd, Edition John Wiley and SonsPublishers, 2011.
2	Samir Palnitkar	Verilog HDL A guide to Digital Design and Synthesis 2nd Edition, Pearson Education, 2017.
3	Reference Manual	Zynq UltraScale+ Device Technical Reference Manual.

Practical: Only for CIE

1. 4–bit Adder/Subtractor using 4-bit carry look Ahead adder with Carry and Overflow indication.
2. 4 – bit Array Multiplier.
3. n-bit Magnitude comparator cascading 1- bit Comparator cell (Behavioural) in structural description.
4. 8-bit asynchronous and synchronous counter using T-Flip Flop in Structural Description.
5. 8-bit synchronous UP/Down Mod n counter with asynchronous reset using Behavioural Description.
6. 4-bit Universal Shift register using D-Flip Flop in Structural Description.
7. Finite state machine design for a specified application
8. Sequence detector using FSM.

Course Outcomes: The students will be able to

CO1: Select appropriate coding style to write Verilog HDL and implement basic combinational circuits to design digital system component.

CO2: Design combinational circuits using PLDs and discuss the architecture of different FPGAs.

CO3: Design combinational circuits using Verilog HDL and implement on FPGA.

CO4: Design sequential circuits and State Machine using Verilog HDL and implement on FPGA.

CO5: Design data path components using Verilog HDL

CO6: Design selected circuit for a particular application using FPGA. Prepare the report.

VLSI Design

Contact Hours/ Week	:3+0+0(L+P+T/SDA)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total SDA Hours	: 0	SEE Marks :	50
Course Code	: S1LVS02	Course Type:	PCC((PB)

Course Objective: This course enables the students to analyze and design combinational, sequential, memory and BiCMOS circuits.

UNIT- I

Introduction: MOS Structure, MOS system under External Bias, Structure and operation of the MOSFET, MOSFET Current-Voltage Characteristics, MOSFET Capacitance.

MOS Inverters- Static Characteristics: Introduction, Resistive-Load Inverter.

08 Hrs

UNIT- II

Combinational Logic Circuits: Static CMOS inverter, Static behaviour, Propagation delay, Power dissipation, Pseudo NMOS inverter, Static CMOS design, Pass gates, CMOS Transmission Gates, Dynamic CMOS design. Driving Large capacitance.

08 Hrs

UNIT- III

Sequential Logic Circuits: Timing metrics for sequential circuits, Static latches and Registers: The Bi-stability principle, Multiplexer based Latches, Master slave edge triggered registers, Static SR Flip-Flops. Dynamic Latches and Registers: Dynamic Transmission gate Edge triggered registers, C^2MOS, True Single Phase Clock Registers (TSPCR).

08 Hrs

UNIT- IV

Arithmetic Building blocks: Adders, Multipliers, Barrel shifter.

Semiconductor Memories: Memory Classification, Non-Volatile Memory devices. Read-Only Memory (ROM) Circuits,

09 Hrs

UNIT- V

Semiconductor Memories contd.. : Static Read-Write Memory (SRAM) Circuits, Dynamic Read-Write Memory (DRAM) Circuits

BiCMOS Logic Circuits: Introduction, Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.

Chip Input and Output (I/O) Circuits: Introduction, ESD Protection, Input Circuits, Output Circuits and L (di/dt) Noise, On-Chip Clock Generation and Distribution.

09 Hrs

Text Books:

1	Jan M Rabaey, Anantha Chandrakasan, Borivoje Nikolic	Digital Integrated Circuit A Design Perspective, 2nd Edition, PHI, 2016.
2	Sung Mo Kang & YosufLeblebici,	CMOS Digital Integrated Circuits: Analysis and Design, 41th Edition, Tata McGraw-Hill, 2002

Reference Books:

1	Neil Weste and K. Eshragian,	Principles of CMOS VLSI Design: A System Perspective, 2^{nd} Edition, Pearson Education (Asia) Pvt. Ltd. 2000.
2	Adel Sedra and Kenneth C. Smith	Microelectronic Circuits Theory and Applications 7^{th} Edition, Oxford Higher Education, 2017.

Course Outcomes: students will be able to

CO1: Analyze the MOS structure and inverter characteristics

CO2: Analyze and design combinational circuits with different design styles.

CO3: Analyze and design sequential circuits with different design styles.

CO4: Analyze and design arithmetic building blocks and Non-Volatile Memory cells.

CO5: Analyze and design Volatile Memory circuits, BiCMOS circuits & Chip I/O circuits.

CO6: Design course level project for a particular application using Mentor graphics/Cadence and prepare the report.

ARM Microcontroller and its Applications

Contact Hours/ Week	: 3+0+0 (L+P+T/SDA)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total SDA Hours	: 00	SEE Marks :	50
Course Code	: S1LVS03	Course Type:	PCC

Course Objective: To impart the knowledge of Cortex M3 and M4 based Microcontroller Architecture, Exception and Interrupt behavior, Programming and configuring on chip peripherals and interfacing of I/O devices.

UNIT- I

Introduction: Microprocessors and Microcontrollers, Von-Neumann and Harvard Architectures, History of ARM family of processors, Architecture and Features of ARM Cortex M3 and M4 processors. Programmer's model: Operation Modes and States, General purpose Registers, Special function Registers, Behavior of APSR. Pipelining, Pre-fetch unit and Branch target forwarding in ARM cortex M3 and M4 processors. Memory system: Memory map.

09 Hrs

UNIT- II

Memory Format: Memory endianness, data alignment and unaligned data access support, Bit-band operation in ARM Cortex M3 and M4 processors. Embedded Software development-1: Embedded Software Development and compilation flow. Data types in C – programming used for Cortex M4 processors. Introduction to Cortex M3 based Microcontroller: Features, Memory map, basic configuration and programming of GPIO. Interfacing Input output devices to Cortex M3 based Microcontroller-1: LEDs and Switches, C-Programming examples.

08 Hrs

UNIT- III

Instruction set: Operation and addressing modes of MOV instruction, Arithmetic instructions, Logical instructions, Memory access instructions, Program flow control instructions, Shift and rotate instructions, Data conversion instructions, Bit-field processing instructions, compare and test instructions. Use of suffix in instructions. ARM Assembler directives, Assembly level programming examples. Interfacing Input output devices to Cortex M3 based Microcontroller-2: 7-segment Display, Push button keys, mxn matrix keypad. Programming examples (Both assembly and C).

08 Hrs

UNIT- IV

Embedded Software development-2: Program flow (Software Flow).

Exceptions and Interrupts: Overview of Exceptions and Interrupts, Exception types, Vector table and Reset status, Exception entrance sequence, Exception handler execution, Exception return, Interrupt latency, NVIC registers for interrupt control, Exception handlers in C and assembly level programming, Stack Frames, Exceptions entrance and stacking, Exception return and unstacking. Programming Examples (Both assembly and C). System control blocks of Cortex M3 and M4 based Microcontroller: Reset, Brown-out detection and External interrupt inputs.

Peripherals in Cortex M3 and M4 based Microcontroller: Configuration and programming (both assembly and C) Nested Vectored Interrupt Controller (NVIC) and Timers.

08 Hrs

UNIT-V

Configuration and programming (Only C) PWM unit, Watchdog timer, Analog to Digital Converter (ADC), Digital to Analog Converter (DAC), Universal Asynchronous Receiver Transmitter (UART) , SPI and I2C. Interfacing Input output devices to Cortex M3 and M4 based Microcontroller-3: Stepper Motor, DC motor, Opto-coupler, Relay unit, Programming examples (both assembly and C).

09 Hrs

Text Books:

1	Joseph Yiu	The Definitive guide to ARM Cortex M3 and Cortex M4 processor, Elsevier, 3rd Edition, 2013.
2	Cortex-M Technical Reference Manual. revision r1p1	
3	LPC17xx Reference Manual.	

Reference Book:

1	Ming-Bo Lin	An Introduction to Cortex-M3-Based Embedded Systems: Cortex-M3 Assembly Language Programming, Createspace Independent Publishing Platform, 2019.

Course Outcomes: Students will be able to

CO1: Discuss the architecture of ARM cortex M3 and M4.
CO2: Develop the C-program for ARM cortex M3 and M4 based microcontrollers in order to Interface Input and output devices.
CO3: Develop the Assembly level program for ARM cortex M3 and M4 based microcontrollers in order to Interface Input and output devices.
CO4: Discuss the concept of Exceptions and interrupts, and Develop the program to configure External interrupts, NVIC and Timers of ARM cortex M3 and M4 based microcontrollers.
CO5: Develop the program to configure PWM, ADC, DAC and UART of ARM cortex M3 and M4 based microcontroller.

Analog IC Design

Contact Hours/ Week	:3+0+0(L+P+T/SDA)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours	: 00	SEE Marks :	50
Course Code	: S1LVS04	Course Type:	PCC

Course Objective: This course enables the students to analyze and design Analog CMOS ICs for different amplifier topologies.

UNIT – I

Introduction: Introduction to Analog IC design, General concepts - Levels of abstraction, Robustness in Analog design, MOS structure, MOS under external bias, MOSFET: Structure, Threshold voltage, I/V Characteristics, Capacitance. Small signal model.

09 Hrs

UNIT – II

Single stage amplifiers: Common source stage – with resistive load, Diode connected load, current source load, Triode load, Source degeneration. Source follower, Common gate stage, Cascode stage.

08 Hrs

UNIT – III

Differential amplifiers: Single ended differential operation, Basic differential pair, common mode response, Differential pair with MOS loads, Current mirrors: Basic current mirrors, Cascode current mirrors, Active current mirrors.

08 Hrs

UNIT – IV

Frequency response of amplifiers: Miller effect, Association of poles with nodes, CS-stage, Source followers, CG-stage. Feedback: General feedback considerations, Feedback topologies. Two port network models.

08 Hrs

UNIT – V

Operational Amplifier: General considerations, one-stage OP Amps, Two-Stage opamps, Common mode feedback, input range limitations, slew rate, power supply rejection. Stability and Frequency Compensation: General considerations, Multipole systems, Phase margin, Frequency compensation, compensation of two stage op-amps.

09 Hrs

Text Book:

1	Behzad Razavi	Design of Analog CMOS Integrated Circuits 2nd Edition, McGraw Hill Education Private Limited, 2017.

Reference Books:

1	Adel Sedra and Kenneth C. Smith	Microelectronic Circuits Theory and Applications 7th Edition, Oxford Higher Education, 2017.
2	P.R. Gray; P.J. Hurst; S.H. Lewis; R.G. Meyer	Analysis and Design of Analog Integrated circuits, 5th Edition, Wiley, 2009.

Course Outcomes: students will be able to

CO1: Analyze the MOS structure and explain the operation of MOSFET.

CO2: Analyze and design single stage CMOS amplifiers with different loads.

CO3: Analyze and design differential amplifiers and current mirrors with different loads.

CO4: Analyze frequency response of amplifiers and discuss the operation of feedback networks.

CO5: Analyze and design operational amplifiers.

Professional Elective-I

ASIC Design

Contact Hours/ Week	: 3 +0+0(L+P+SDA)	Credits:	3.0
Total Lecture Hours	: 42	CIE Marks:	50
Total SDA Hours	: 00	SEE Marks:	50
Course Code	: S1LVSE11	Course Type:	PEC

Course Objective: Design various ASIC configurations, analyze Programmable ASIC memories, and Use CAD tools for ASIC design flow.

UNIT- I

Introduction: Types of ASIC Design, ASIC Design Flow, FPGA design Flow, Programmable logic device, ASIC cell libraries.

09 Hrs

UNIT- II

Data Logic Cells: Data Path Elements, Adders, Multiplier, Arithmetic Operator, I/O cell. **ASIC Library Design**: Logical effort: practicing delay, logical area and logical efficiency logical paths, multi stage cells, optimum delay, optimum no. of stages, library cell design.

08 Hrs

UNIT- III

Low-Level Design Entry: Schematic Entry, **Programmable ASIC**: Anti-fuse, Static RAM, EPROM and EEPROM Technology, FPGA, Programmable ASIC logic cells, ASIC I/O cells, Programmable ASIC Interconnects.

08 Hrs

UNIT- IV

A Brief Introduction to Low Level Design Language: introduction to EDIF, PLA Tools and CFI designs representation. Half gate ASIC. Introduction to Synthesis and Simulation.

ASIC Construction: Physical Design, CAD Tools, System Partitioning, Estimate ASIC size, FPGA Partitioning and its Methods.

08 Hrs

UNIT- V

Floor Planning and Placement and Routing: Physical Design, System Partitioning, Estimating ASIC size, partitioning methods. Floor planning tools, I/O and power planning, clock planning, placement algorithms. Global Routing, Local Routing, Detail Routing, Special Routing, Circuit Extraction and DRC.

09Hrs

Text Books:

1	M.J.S .Smith	"Application - Specific Integrated Circuits" – Pearson Education, 2003.
2	Jose E.France, YannisTsividis	"Design of Analog-Digital VLSI Circuits for Telecommunication and signal processing", 2nd Edition, Prentice Hall, 1993.
3	MalcolmR.Haskard; Lan. C. May	"Analog VLSI Design – NMOS and CMOS", Prentice Hall, 1998.
4	Mohammed Ismail and Terri Fiez	"Analog VLSI Signal and Information Processing", McGraw Hill, 1994.

Course Outcomes: Students will be able to

CO1: Identify and apply appropriate ASIC configuration for particular application.

CO2: Select and apply appropriate techniques to optimize data path and arithmetic components.

CO3: Identify and use Programmable ASIC memories according to design requirements.

CO4: Analyze the synthesis process of ASICs.

CO5: Analyze physical design process flow.

VLSI Design Automation

Contact Hours/ Week	: 3+0+0 (L+P+SDA)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total SDA Hours	: 00	SEE Marks :	50
Course Code	: S1LVSE12	Course Type:	PEC

Course Objective: To impart knowledge on implementation of automation methods for VLSI physical design.

UNIT- I

Logic Synthesis & Verification: Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

VLSI Automation Algorithms: Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

09 Hrs

UNIT- II

Placement, Floor Planning & Pin Assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment**.**

08 Hrs

UNIT- III

Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches.

08 Hrs

UNIT- IV

Detailed Routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

Over The Cell Routing & Via Minimization: two layers over the cell routers, constrained & unconstrained via minimization.

08 Hrs

UNIT- V

Scripting Languages: Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables. Inter process Communication Threads, Compilation & Line Interfacing.

09 Hrs

Text Books:

1	NaveedShervani	Algorithms for VLSI physical design Automation, Kluwer Academic Publisher, 3rd Edition, 2013
2	ChristophnMeinel & Thorsten Theobold	Algorithm and Data Structures for VLSI Design, KAP, 2002.
3	Rolf Drechsheler	Evolutionary Algorithm for VLSI, Springer, 2nd Edition, 2013.
4	Randal L, Schwartz Tom Phoenix	Learning PERL, Oreilly Publications, 6th Edition, 2011.

Course Outcomes: Students will be able to,

CO1: Identify and discuss partitioning algorithms used to design VLSI automation and describe the basic concepts of Logical high level synthesis and verification of hardware models

CO2: Discuss the placement and floor planning algorithms.

CO3: Select suitable routing algorithms in VLSI design automation.

CO4: Discuss routing algorithms with respect to different layers.

CO5: Discuss script languages for VLSI design automation.

VLSI for Digital Signal Processing

Contact Hours/ Week	: 3 +0+0(L+P+T)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours	: 00	SEE Marks :	50
Course Code	: S1LVSE13	Course Type:	PEC

Course Objective: Design custom or semi-custom VLSI circuits for Signal Processing applications.

UNIT- I

Introduction: DSP algorithms: FIR and IIR Filters, Representation of DSP Algorithms.

Iteration Bounds: loop bound and Iteration bound, Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs.

09 Hrs

UNIT- II

Pipelining and parallel processing: pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power.

Retiming: Properties, Solving Systems of Inequalities, Retiming techniques.

08 Hrs

UNIT- III

Unfolding: Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Applications of Unfolding.

08 Hrs

UNIT- IV

Systolic architecture design: systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design.

08 Hrs

UNIT- V

Fast convolution–Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution,

Pipelined and Parallel recursive filter: Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing.

09 Hrs

Text Book		
1	KeshabK.Parhi	“VLSI Digital Signal Processing systems, Design and implementation ", Wiley, Inter Science, 1999.

Reference Books:		
1	Mohammed Isamail and Terri Fiez	Analog VLSI Signal and Information Processing, Mc Graw-Hill, 1994.
2	S.Y. Kung, H.J. White House, T. Kailath	VLSI and Modern Signal Processing, Prentice Hall, 1985.
3	Jose E. France, YannisTsividis	Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing, Prentice Hall, 2nd Edition, 1994.

Course Outcomes: The students will be able to

CO1: Discuss various DSP algorithms and represent using block diagrams, signal flow graphs and data flow graphs.

CO2: A. Compute the iteration bound using Longest Path Matrix Algorithm and the Minimum Cycle Mean Algorithm.

B. Calculate critical path computation time and power consumption in filters

CO3: Perform retiming in filters and select different retiming techniques and algorithm for unfolding.

CO4: Discuss Systolic architecture design methodologies

CO5: Apply various algorithms for efficient implementation of convolution and implement filters using pipelining and parallel processing.

Professional Elective-II

Data Structures

Contact Hours/ Week	: 3+0+0(L+P+T)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Practical Hours	: 00	SEE Marks :	50
Course Code	: S1LVSE21	Course Type:	PEC

Course Objective: Enable students to implement different data structures using C.

UNIT- I

Structures and Unions: Defining a Structure, declaring Structure variables, accessing Structure members, Structure initialization, copying and comparing Structure variables, and operations on individual members, array of Structures, array within Structure, Structure within Structure, Structures and Functions, Unions, size of structures. File management in C: Defining and Opening a file, Closing a file, Input/output operations on files - getc(), putc(), getw(), putw(), fscanf(), fprintf(), Error handling during I/O operations - feof(), ferror(), Random access to files - ftell(), rewind(), fseek(), Command line arguments.

09 Hrs

UNIT- II

The Stack: Definition and Examples, representing Stacks in C, Example: Infix, Postfix, and Prefix.

Recursion: Recursive Definition and Processes, Recursion in C.

Queues: The Queue and Its Sequential Representation: C implementation of Queues, Insertion, Deletion and Display operations, Types of Queues (Linear and Circular Queues) Self-Study: Priority and Double Ended Queues.

08 Hrs

UNIT- III

Dynamic memory allocation: malloc(), calloc(), realloc(), free().

Linked lists: Inserting and removing nodes from a list, linked implementation of stacks, getnode and freenode operations, linked implementation of queues, examples of list operation, list implementation of priority queues, header nodes.

Lists in C: allocating and freeing dynamic variables, linked lists using dynamic variables, queues as lists in C, examples of list operations in C, non-integer and non-homogeneous lists, implementing header nodes.

08 Hrs

UNIT- IV

Other List Structures: Circular lists, stack as a circular list, queue as a circular list, primitive operations on circular lists, doubly linked lists, Primitive operations on doubly linked list.

08 Hrs

UNIT- V

Trees: Operations on Binary Trees, Applications of Binary Trees, and Binary Tree Representations: Node representation of Binary Trees, Internal and External Nodes, Implicit array representation of Binary Trees, Binary Tree Traversals in C. Trees and Their applications:

C Representations of Trees, Tree Traversals, General Expressions as Trees, Evaluating an Expression Tree, Constructing a Tree.

09 Hrs

Text Books:

1	Yashavant Kanetkar	Data Structures Through C, BPB publications, 4th Edition, 2022.
2	E. Balagurusamy	Programming in ANSI C, 3rd Edition, TMH, 2018.
3	Yedidyah Langsam, Moshe J. Augenstein, Aaron M. Tenenbaum	Data structures using C and C++, PHI, 2nd Edition, 2015.

Course outcomes: On successful completion of this course, students will be able to:

CO1: Apply advanced C programming techniques like pointers, structures, union and files to develop solutions for a given problem.
CO2: Discuss and implement different linear data structures like stacks and queues using static memory allocation technique.
CO3: Discuss different types of linked lists and implement using dynamic memory allocation technique.
CO4: Discuss non-linear data structures like trees and implement using dynamic memory allocation technique.
CO5: Apply the knowledge of stacks, queues, linked lists and trees to design and develop solutions to given problems.

Low Power VLSI Design

Contact Hours/ Week	: 3+0+0(L+P+T)	Credits:	3.0
Total Lecture Hours	: 42	CIE Marks:	50
Total Tutorial Hours	: 00	SEE Marks:	50
Course Code	: S1LVSE22	Course Type:	PEC

Course Objective: Analyze and estimate power at different abstraction levels of CMOS VLSI circuits.

UNIT- I

Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices. **Device & Technology Impact on Low Power:** Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

09 Hrs

UNIT- II

Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.

08 Hrs

UNIT- III

Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

Low Power Design Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library.

08 Hrs

UNIT- IV

Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. **Low power Architecture & Systems:** Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

08 Hrs

UNIT- V

Low power Clock Distribution, **Algorithm & Architectural Level Methodologies:** Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

09 Hrs

Text Books:

1	Kaushik Roy, Sharat Prasad	"Low-Power CMOS VLSI Circuit Design" Wiley, 2009
2	Gary K. Yeap	"Practical Low Power Digital VLSI Design", KAP, 2008.
3	Rabaey, Pedram	"Low Power Design Methodologies" Kluwer Academic, 2009.

Course Outcomes: Students will be able to

CO1: Analyze the impact of low power in VLSI circuits.

CO2: Recognize Role of simulation possible at various levels of design.

CO3: Describe the relationship of probability while calculating power dissipation of circuits.

CO4: Apply power reduction techniques at circuit and architectural level.

CO5: Discuss different clock distribution techniques in low power VLSI design.

VLSI Testing and Verification

Contact Hours/ Week	: 3+0+0(L+P+T)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Practical Hours	: 00	SEE Marks :	50
Course Code	: S1LVSE23	Course Type:	PEC

Course Objective: Enable students to understand fault model and generate test vectors for digital circuits and discuss various verification tools.

UNIT- I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing. **Faults:** Single Stuck at faults, Temporary Faults. Bridging faults, Transient faults.
Fault modeling: Fault equivalence, dominance and collapsing.
Fault Simulation: parallel, concurrent and deductive simulation.

09Hrs

UNIT- II

Test Generation for Combinational Logic Circuits: Test Generation Techniques for Combinational Circuits: Truth table method, Fault matrix method, Boolean difference method, Path sensitization method, D-Roth algorithm, PODEM and FAN. Detection of Multiple Faults in Combinational Logic Circuits.

08 Hrs

UNIT- III

Design of Testable Sequential Circuits: Controllability and Observability, Ad Hoc Design Rules for Improving Testability, The Scan-Path Technique for Testable Sequential Circuit Design, Level-Sensitive Scan Design, Random Access Scan Technique, Partial Scan, Testable Sequential Circuit Design Using Nonscan Techniques, Crosscheck, Boundary Scan.

08 Hrs

UNIT- IV

Built-In Self Test: Test Pattern Generation for BIST, Output Response Analysis, BIST Architectures-BILBO.
Testable Memory Design: RAM Fault Models, Test Algorithms for RAMs: March algorithm(Row, Column), galloping algorithm, butterfly algorithm, Neighbourhood Pattern Sensitive Faults(NPSF), Detection of Pattern Sensitive Faults, BIST Techniques for Ram Chips, Test Generation and BIST for Embedded RAMs.

08 Hrs

UNIT- V

Importance of Design Verification: The importance of verification, Reconvergence model, Formal verification, Assertion based verification, Equivalence checking, model checking, and functional verification.
Verification Tools: Linting tools: Limitations of linting tools, lintingverilog source code, linting VHDL source code, lintingOpenVera and e-source code, code reviews.
Simulators: Stimulus and response, Event based simulation, cycle based simulation, Co-simulators, verification intellectual property: hardware modelers, waveform viewers.

Verification plan: The role of verification plan: specifying the verification plan, Levels of verification: unit level verification, reusable components verification, ASIC and FPGA verification, system level verification, board level verification.

09 Hrs

Text Books:

1	P. K. Lala	Digital Circuit Testing and Testability, Academic Press, 1997.
2	M.L. Bushnell and V.D. Agrawal	Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Springer, 1st Corrected Edition 2002, Corr. 2nd printing 2004.

Course Outcomes: Students will be able to

CO1: Identify and generate test for the faults in digital circuits. Identify and apply the appropriate test generation technique for combinational circuits.
CO2: Identify and apply the appropriate Ad Hoc techniques to improve testability of sequential circuits.
CO3: Select appropriate algorithms to test memory elements.
CO4: Discuss verification plan and verification tools.
CO5: Analyze the circuits for static timing verification. Design software algorithm or hardware circuit to test the IC. Prepare report on the same.
CO6: Design the circuit for a particular application using appropriate tool. Prepare the report.

Embedded Systems Lab

Lab work Hours/Week	: 0+4+0 (L+P+T)	Credits :	2.0
Total Lecture Hours Total Lab Hours	: 00 : 56	CIE Marks :	50
		SEE Marks :	50
Course Code	S1LVSL1	Course Type:	PCCL

Course Objectives: Enable students to develop assembly level and C-program for Cortex M3 based microcontrollers to interface input- output devices by configuring on chip peripherals.

List of Experiments –evaluation board:

1. Develop a system to implement a calculator which can perform the operations such as addition, subtraction, Logical AND and Logical OR using 4x4 matrix Keypad/Switches and 16x2 LCD/LEDs interfaced to Cortex M3 based microcontroller. (matrix Keypad, LCD/LED)
2. Develop a system to implement a Traffic control system using on-chip timer and LEDs/7-segment Displays interfaced to Cortex M3 based microcontroller. (Timer, LEDs/7-segment Display)
3. Develop a system to implement a Temperature control system using temperature sensor, on-chip ADC and LCD interfaced to Cortex M3 based microcontrollers. (Signal conditioning circuit, ADC, / LCD, Relay)
4. Develop a system to measure/control the rotation speed of a DC motor using on-chip timer/PWM module of Cortex M3 based microcontroller. (PWM, DC motor, Switches)
5. Develop a system to control the direction of rotation and speed of rotation of Stepper motor interfaced to Cortex M3 based microcontroller. (Stepper motor, Switches/ Push button keys)
6. Develop a system to measure the frequency of the input signal/rotation speed of a DC motor interfaced to Cortex M3 based microcontroller. (DC motor, Opto coupler, Timer, LCD)
7. Develop a system to control the bottle filling system using Cortex M3 based microcontrollers. (Stepper motor, IR sensors/Proximity, Solenoid valve)
8. Develop a system to control the Elevator system using Cortex M3 based microcontrollers. (Stepper Motor, Proximity sensor, 7segement Display, Push button keys).
9. Develop a weighing machine using Cortex M3 based microcontrollers. (Signal Conditioning circuit, Load cell, ADC, LCD).
10. Develop a Real time clock using Cortex M3 based Microcontroller. (LCD, Timer).

Open ended Experiments:

1. Develop a Washing machine control unit using Cortex M3 based microcontrollers. (LED, Multiplexed 7-segment display, Keypad, Solenoid valve, Motor control (ON/OFF + Speed), Control logic).

Course Outcomes: Students will be able to

CO1: Develop, debug and execute embedded C and Assembly level programs to interface input/output devices to Cortex M3 based microcontroller.

CO2: Develop, debug and execute embedded C and Assembly level program – Program to configure On-chip peripherals of Cortex M3 based microcontroller.

CO3: Develop, debug embedded System applications using Cortex M3 based microcontroller.

SIDDAGANGA INSTITUTE OF TECHNOLOGY, TUMAKURU-03

(An autonomous Institute under Visvesvaraya Technological University)

SCHEME OF TEACHING AND EXAMINATION

II SEMESTER M.Tech. VLSI Design and Embedded Systems

II SEMESTER												
					Teaching Hours /Week			**Examination**				**Credits**
			Course Code	**Course Title**	**Theory**	**Practical/ Seminar**	**Tutorial/ Skill Development Activities**	**Duration in hours**	**CIE Marks**	**SEE Marks**	**Total Marks**	
					L	P	T/SDA					
1	IPCC	PCC/ PEC/ MDC/ PCC (PB) /IPCC	S2LVSI01	Real time operating systems	3	2	0	03	50	50	100	4
2	PCC		S2LVS02	Semiconductor Process Technology	3	0	0	03	50	50	100	3
3	PCC(PB)		S2LVS03	Design of IoT Systems	3	0	0	03	50	50	100	3
4	PEC		S2LVSE3x	Professional Elective – III	3	0	0	03	50	50	100	3
5	PEC		S2LVSE4x	Professional Elective – IV	3	0	0	03	50	50	100	3
6	PCCL	PCC L	S2LVSL1	VLSI Design Lab	0	4	0	03	50	50	100	2
7		AEC/ SEC	S2LVSA20x	Ability/Skill Enhancement Course (Offline/Online)	00 01	02 00	--- ---	03	50	50	100	1
TOTAL					**16**	**08**	**0**	**21**	**350**	**350**	**700**	**19**

Note: **PCC:** Professional core. **IPCC**-Integrated Professional Core Courses, **PCC(PB):** Professional Core Courses (Project Based), **PCCL**-Professional Core Course lab, **PEC**- Professional Elective Courses, **MDC**- Multi-Disciplinary Courses, **L-Lecture, P-Practical, T/SDA-Tutorial / Skill Development Activities** (Hours are for Interaction between faculty and students) **L-Lecture, P-Practical, T/SDA-Tutorial / Skill Development Activities** (Hours are for Interaction between faculty and students) **PBLC**: Project Based Learning Course,

Note: **xxx** means specialization code for example **MDE- Design** Engineering, **LDN**- Digital Communication and Networking, **SCE**- Computer Engineering, **CCT**- Construction Technology, **AUD**- Urban Design, **MBA**- Master of Business Administration, **MCA**-Master of Computer Application, etc.

Ability Enhancement Courses (AEC):. These courses are designed to help students enhance their skills in communication, language, and personality development. They also promote a deeper understanding of subjects like social sciences and ethics, culture and human behaviour, human rights, and the law. Skill Enhancement Course (SEC): Skill Enhancement Course means a course designed to provide value-based or skill-based knowledge and should contain both theory and lab/hands-on/training/fieldwork. The main purpose of these courses is to provide students with life skills in the hands-on mode to increase their employability. If AEC/SEC courses are ONLINE (MOOCs) courses suggested by the concerned board of studies. These courses will be made available on www. online.vtu.ac.in, however online courses are not considered for vertical progression, but qualifying in online courses is mandatory for the award of the degree.

Professional Elective - III		Professional Elective - IV	
Course Code	**Course Title**	**Course Code**	**Course Title**
S2LVSE31	CMOS RF Circuit Design	S2LVSE41	System on Chip Design
S2LVSE32	Mixed Signal Circuit Design	S2LVSE42	System Verilog
S2LVSE33	Nano Electronics	S2LVSE43	RISC-V Processor Design
S2LVSE34	Design of CMOS Phase Locked Loops	S2LVSE44	Static Timing Analysis
S2LVSE35	Hardware Security Systems		

Ability / Skill Enhancement Courses				
Course Code	**Course Title**	**L**	**P**	**T/SDA**
S2LVSA201	Peripheral and IO Firmware development	0	2	0
S2LVSA202	Machine learning for Embedded Systems	0	2	0
S2LVSA203	Data analytics using R-programming.	0	2	0
PCC/PCCL/IPCC/PEC/MDC/PCC (PB): These are the courses which will suit the individual specializations				

Real Time Operating Systems

Contact Hours/Week	: 3+2+0 (L+P+T/SDA)	Credits :	4.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Lab Hours	: 28	SEE Marks :	50
Course Code	: S2LVSI01	Course Type:	IPCC

Course Objectives: To design and develop embedded applications using real-time operating systems.

UNIT- I

Introduction to operating systems: Operating systems structure: simple structure, layered approach, Micro kernels, modules Introduction to Real Time Systems, Embedded Systems.
Real Time System Resources: Resource Analysis, Real-Time Service Utility, Real-Time OS, Thread Safe Reentrant Functions.
Process: Necessary and Sufficient feasibility condition , Preemptive Fixed-Priority Policy
Scheduling algorithms: FCFS, Priority and Round Robin scheduling

09 Hrs

UNIT- II

Process: Rate Monotonic , Deadline Monotonic scheduling, Dynamic priority policies.
I/O Resources: Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture.
Memory: Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash file systems.

08 Hrs

UNIT- III

Multi-resource Services: Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion.
Soft Real-Time Services: Missed Deadlines, QOS.
Soft Real-Time Services: Alternatives to rate monotonic policy, mixed hard and soft real-time services.
Embedded System Components: Embedded system components of Real time stereo vision system monitoring.

08 Hrs

UNIT- IV

Firmware Components: The 3 firmware components, RTOS system software mechanisms, Software application components.
Debugging Components: Exceptions, assert, Checking return codes. Single-step debugging, kernel scheduler traces, Test access ports, Trace ports, Power-On self test and diagnostics, External test equipment, Application-level debugging.
Performance Tuning: Basic concepts of drill-down tuning, hardware – supported profiling and tracing, Building performance monitoring into software, Path length, Efficiency Call frequency, Fundamental optimizations.

08 Hrs

UNIT- V

High availability and Reliability Design: Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design tradeoffs, Hierarchical applications for Fail-safe design.

Process and Threads: Process and thread creations, Programs related to semaphores, message queue, shared buffer applications involving inter task/thread communication

09 Hrs

Reference Books:

1	Sam Siewert	"Real-Time Embedded Systems and Components" Cengage Learning India Edition, 2016.
2	Myke Predko	"Programming and Customizing the PIC microcontroller" 3rd Ed, TMH, 2008.
3	Jhon Wiley	"Programming for Embedded Systems" Dreamtech Software Team, Jhon Wiley, India Pvt. Ltd, 2008.
4	Abraham S ilberschatz, Peter Baer Galvin, Greg Gagne	Operating system concepts, Wiley India, 9th Edition, 2013.
5	Pof Prof. Rajib Mall	NPTEL course Real Time Systems, IIT Kharagpur,

Practicals for CIE

1. Creation of multiple process/threads
2. Assigning different priorities to process/threads
3. Threads with same priority and Priority Inheritence
4. Communication between Parent and child thread.
5. Shared recourse and Semaphore to manage shared recourse
6. Communication between a pipe server and a process thread
7. PROSIX based message Queue
8. Real time Camera interfacing.
9. Arduino programming for sensor interfacing using freeRTOS

Course Outcomes: The student will be able to

CO1: Discuss the fundamental concepts of real-time operating systems.
CO2: Analyze the system resources required to build RTOS.
CO3: Analyze the Multi-service resources required for RTOS
CO4: Analyze various performance tuning techniques
CO5: Develop programs for multithreaded applications using suitable techniques.
CO6: Develop C programs to create multithreads and demonstrate the Working and prepare the report.

Semiconductor Process Technology

Contact Hours/ Week	: 3+0+0 (L+P+SDA)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Practical Hours	: 0	SEE Marks :	50
Course Code	: S2LVS02	Course Type:	PCC

Course objective: This course aims at understanding the manufacturing methods and their underlying scientific principles in the context of technologies used in VLSI chip fabrication.

UNIT- I

Introduction: Electronic-Grade Silicon, Czochralski Crystal Growing, Float Zone Crystal Growing, Silicon Shaping, Process Considerations. Environment for VLSI technology: clean room and safety requirements, Wafer cleaning process.

Epitaxy: Introduction, Vapour-Phase Epitaxy, Molecular Beam Epitaxy, Epitaxial Evaluation.

Oxidation: kinetics of silicon dioxide growth for thick, thin and ultra-thin films. Oxidation technologies in VLSI and ULSI; Characterization of oxide films.

08 Hrs

UNIT- II

Chemical Vapour deposition techniques: CVD (PECVD, APCVD, LPCVD and ALD) techniques for deposition of materials.

Metallization: Metallization Applications, Metallization Choices, Physical Vapor Deposition (evaporation and sputtering techniques). Contact, Via, and Passivation, .Failure mechanisms in metal interconnect; multilevel Metallization schemes.

08 Hrs

UNIT- III

Impurity incorporation: Models of **Diffusion** in Solids, Fick's laws for Diffusion, Measurement Techniques, Fast Diffusion in Silicon.

Ion implantation: Introduction, Range Theory, Implantation Equipment, Annealing, Shallow Junctions, High-Energy Implantation, annealing; Characterization of impurity profiles.

Reactive Plasma Etching: Introduction, Plasma Properties, Feature-Size Control and Anisotropic Etch Mechanisms, Other Properties of Etch Processes, Reactive Plasma-Etching Techniques and Equipment, Specific Etch Processes.

09 Hrs

UNIT- IV

Lithography: Introduction, Positive and Negative photoresists, Optical Lithography, Electron Lithography, X-ray Lithography, Ion Lithography.

Thin film Characterization: Overview of thin film characterization, **Structural** properties: Optical Profiler Scanning electron microscopy (SEM), TEM, AFM, X-ray diffraction (XRD), **Electrical** properties: Resistance/resistivity – four point probe, Vander Pauw, **Mechanical** properties: Stress-curvature measurements**.**

09 Hrs

UNIT- V

VLSI Process Integration: Introduction, Fundamental Considerations for IC Processing, NMOS IC technology, CMOS IC Technology, FF,SS, & TT processes of CMOS. MOS Memory IC Technology, Introduction to Embedded Non-Volatile Memory (eNVM) fabrication.

Packaging of VLSI Devices: Introduction, Package Types, Packaging Design Considerations and Flip chip packaging.

08 Hrs

Text Books:

1	S. M. Sze,	VLSI Technology, McGraw-Hill, 2nd Edition, 2017.
2	S.K. Ghandhi,	VLSI Fabrication Principles, John Wiley Inc., New York, 2nd Edition, 2008.

Reference Books:

1	John A. Venables	Introduction to Surface and Thin Films Processes, Cambridge University Press, 2010.
2	Leon I. Maissel and Reinhard Glang.	Handbook of Thin Film Technology, McGraw-Hill Publishing Company, New Delhi (1970)

Course Outcomes: students will be able to

CO1: Analyze the crystal growth process and select appropriate epitaxial growth techniques for IC's fabrication.

CO2: Analyze and Select appropriate deposition method to deposit various material in the thinfilm for IC's fabrication.

CO3: Identify and select appropriate impurity incorporation, and etching methods used in IC's fabrication

CO4: Describe the various lithography techniques used in IC's fabrication. Analyze the material properties of thin films using the various characterization techniques.

CO5: Apply various process sequences and special considerations for IC's fabrication. Select an appropriate package type and explain design considerations of VLSI devices.

Design of IoT Systems

Contact Hours/ Week	: 3 +0+0 (L+P+SDA)	Credits:	3.0
Total Lecture Hours	: 42	CIE Marks:	50
Total SDA Hours	: 0	SEE Marks:	50
Course Code	: S2LVS03	Course Type:	PCC (PB)

Course Objective: This course aims at understanding IoT Communication Technologies and developing software required for the design of IoT systems.

UNIT- I

Characteristics of IoT, IoT architectures and Reference Models, A core IoT functional Stack, Data management and Compute stack. Introduction to the IoT Framework: A brief refresher on the Internet, Communication models and Communication APIs, The IoT Framework, Types of IoT Systems, Challenges of implementing Effective IoT Systems. IoT Levels and Deployment Templates.

08 Hrs

UNIT- II

IoT Physical Devices and End points: Introduction to Renesas Synergy kits, Arduino and Raspberry pi boards. Introduction to Sensors, Actuators and Smart objects/sensors, IoT Design methodology.

IoT Connectivity Technologies: IEEE 802.15.4, Zigbee, Thread, ISA 100.11A, Wireless HART, RFID, NFC, DASH7, Z-Wave, Weightless, Sigfox, LoRA, NB-IoT, Wifi, Bluetooth (Text Book 1: Chapter 7)

08 Hrs

UNIT- III

IoT Communication Technologies: Infrastructure Protocols – Internet Protocol version 6,6LowPAN, QUIC, Micro Internet Protocol, Nano Internet Protocol, Data Protocols – MQTT, MQTTSN, CoAP, AMQP, XMPP, SOAP, REST, WebSocket Identification Protocols.

08 Hrs

UNIT- IV

IoT Application Transport Methods: Application Layer not present, SCADA, Generic Web based Protocols, IoT Application Layer Protocols (Text Book 2: Chapter 6)

Securing IoT: Common Challenges in OT Security – Erosion of Network Architecture, Pervasive Legacy Systems, Insecure Operational Protocols, Other Protocols, Device Insecurity, Dependence on External Vendors, How IT and OT Security Practices and Systems vary, Formal Risk Analysis Structures: OCTACE and FAIR, The Phased Application of Security in an Operational Environment (Text Book 2: Chapter 8)

09 Hrs

UNIT- V

Case Studies for IoT: Agricultural IoT (Text Book 1: Chapter 12) Vehicular IoT (Text Book 1: Chapter 13) Health Care IoT(Text book 1: Chapter 14) Paradigms, Challenges and Future:

Evolution of new IoT paradigms, Challenges Associated with IoT, Emerging pillars of IoT (Text book 1: Chapter 15)..

09 Hrs

Text Books:

1	Misra S, Mukherjee A, Roy A.	Introduction to IoT. Cambridge University Press; 2021 Jun 10.
2	David Hanes, Gonzalo Salgueiro,Patrick Grossetete, Robert Barton, Jerome Henry	IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things, Pearson Education (Cisco Press Indian Reprint), (ISBN: 978- 9386873743), 1st Edition, 2018.
3	Sammi salama hussen Hajjaj, Kisheen Rao Gsangaya	The Intenet of Mechanical Things: The IoT Framework for Mechanical Engineers., CRC press Taylor and Francis Group, 1st Edition 2022,
4	Srinivasa K Srinivasa K.G., Siddesh G.M., Hanumantha Raju R.	Internet of Things, Cengage learning India 1st Edition, 2018.
5	Arshdeep Bahga, Vijay Madisetti	Internet of Things , A Hands on Approach 1st Edition, 2015.

Course Outcomes: Students will be able to
CO1: Discuss the building blocks of an IoT system.
CO2: Describe the IoT Design methodology and the operation of end point devices.
CO3: Discuss the operation of IoT Communication Technologies
CO4: Describe the IoT Application Transport Methods and Securing IoT
CO5: Prepare case studies and develop IoT based system.

Professional Elective – III

CMOS RF Circuit Design

Contact Hours/ Week	: 3+0+0(L+P+T)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours	: 00	SEE Marks :	50
Course Code	: S2LVSE31	Course Type:	PEC

Course Objective: To impart the knowledge on designing CMOS RF Circuit.

UNIT- I

Introduction to RF Design and Wireless Technology: Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Intersymbol interference, random processes and noise, Sensitivity and dynamic range, conversion of gains and distortion, characteristics of passive IC components, resistor, capacitor and inductor.

09 Hrs

UNIT- II

RF Modulation: Analog Modulation: Amplitude Modulation, Phase and Frequency Modulation, Digital modulation: Basic concepts, Binary Modulation, Quadrature Modulation. Power efficiency of modulation schemes, Coherent and Non-coherent detectors. Mobile RF communication, basics of multiple access techniques and wireless standards.

08 Hrs

UNIT- III

Transceiver Architectures: Receiver Architecture: Heterodyne, Homo dyne, Image Reject Receiver and Transmitter Architecture.

Distributed Systems: Transmission lines, reflection coefficient, the wave equation, examples, Lossy transmission lines, Smith charts – plotting gamma.

High Frequency Amplifier Design: Bandwidth estimation using open-circuit time constants, Bandwidth estimation using short-circuit time constants, Rise time, delay and bandwidth, Zeros to enhance band width, Shunt-series amplifiers, tuned amplifiers, and Cascaded amplifiers.

08 Hrs

UNIT- IV

Low noise Amplifier design: CS stage: Inductive load, Resistive Feedback, Inductive degeneration. Variants of CS LNA, Noise – Cancelling LNAs, Differential LNAs. Non linearity Calculations in LNAs.

Mixers: Mixer Nose Figures, Port – Port Feed through, Single –balanced and double balanced Mixers, Introduction to Passive and Active Mixers.

08 Hrs

UNIT- V

Oscillators: General Principles: Feedback view, One-Port view, Cross- Coupled Oscillator, Three – Point Oscillators. Voltage Controller Oscillators (VCO): Tuning Limitations, Effect of varactor Q, VCOs with wide tuning Range. Effect of Phase Noise, Low noise VCOs.

Phase Locked Loop (PLL): Type – I PLLs: VCO phase Alignment, Dynamics of Type – 1 PLLs, Frequency Multiplication, drawbacks of Type – 1 PLL. Type-II PLLs: Phase/Frequency Detectors, Charge Pumps, Charge-Pump PLLs, Transient Response.
Integer N Frequency Synthesizer: Basic integer N Frequency Synthesizer, Setting behavior, Spur reduction technique.

09 Hrs

Text Books:

1	B. Razavi	RF Microelectronics, PHI, 2nd Edition, 2011
2	R. Jacob Baker, H.W. Li, D.E. Boyce	CMOS Circuit Design, layout and Simulation, PHI, 2nd Edition, 2004.
3	Thomas H. Lee	Design of CMOS RF Integrated Circuits, Cambridge University press, 2nd Edition, 2003.
4	Y.P. Tsividis	Mixed Analog and Digital Devices and Technology, TMH, 2010

Course Outcomes: Students will be able to,
CO1: Discuss the performance parameters to be considered for the design of RF circuits.
CO2: Identify, select and describe the modulations technique and RF communication concepts for RF circuit design.
CO3: Discuss various Transceiver architecture and bandwidth estimation techniques.
CO4: Identify and discuss the general considerations of low noise amplifiers and concepts of mixers.
CO5: Discuss the modeling of various devices at RF Frequency and general principles of oscillators and PLL. Design RF modulation modules and various amplifiers using Matlab Simulink. Prepare the report.

Mixed Signal Circuit Design

Contact Hours/ Week	: 3+0+0(L+P+T)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours	: 00	SEE Marks :	50
Course Code	: S2LVSE32	Course Type:	PEC

Course objective: Enable students to understand the various integrated based filters, data converters, integrated circuit of oscillators and PLLs in IC design.

UNIT- I

Submicron CMOS Circuit Design

Submicron CMOS: Overview and Models, CMOS process flow, Capacitors and Resistors. Digital circuit design: The MOSFET Switch, Delay Elements, An Adder. Analog Circuit Design: Biasing, Op-Amp Design, Circuit Noise.

09 Hrs

UNIT- II

Integrator Based CMOS Filters

Integrator Building Blocks- low pass filter, Active RC integrators, MOSFET-C Integrators, gm-C integrators, discrete time integrators. Filtering Topologies: The Bilinear transfer function, The Biquadratic transfer function, Filters using Noise shaping.

08 Hrs

UNIT- III

Data Converter Architectures

DAC Architectures- Resistor string, R-2R ladder Networks, Current Steering, Charge Scaling DACs, Cyclic DAC, and Pipeline DAC. ADC Architectures- Flash, Two-step flash ADC, Pipeline ADC, Integrating ADC‘s, Successive Approximation ADC.

08 Hrs

UNIT- IV

Data Converter Modeling and SNR

Sampling and Aliasing: modeling approach, Impulse sampling, The sample and Hold, Quantization noise. Data converter SNR: An overview, Clock Jitter, Improving SNR using Averaging, Decimating filter for ADCs, Interpolating filter for DACs, Band pass and High pass sinc filters - Using feedback to improve SNR.

08 Hrs

UNIT- V

Oscillators and PLL

LC oscillators, Voltage Controlled Oscillators. Simple PLL, Charge pumps PLLs, Non ideal effects in PLLs, Delay Locked Loops.

09 Hrs

Course Outcomes: students will be able to
CO1: Describe the concepts for mixed signal MOS circuit.
CO2: Analyze the characteristics of IC based CMOS filters.
CO3: Design various data converter architecture circuits.
CO4: Analyze the signal to noise ratio and modeling of mixed signals.
CO5: Design oscillators and phase lock loop circuit.

Text Books:

1	R.Jacob Baker	CMOS Mixed Signal Circuit Design, Wiley India, IEEE Press, reprint 2008.
2	R.Jacob Baker	CMOS Circuit Design, Layout and Simulation, Wiley India, IEEE Press, 2nd Edition, reprint, 4th Edition, 2019.
3	Behzad Razavi	Design of Analog CMOS Integrated Circuits, McGraw Hill, 2nd Edition, 2017.

Nano Electronics

Contact Hours/ Week	: 3+0+0(L+P+T)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours	: 00	SEE Marks :	50
Course Code	: S2LVSE33	Course Type:	PEC

Course Objective: Enable students to understand various advanced concepts in nanoelectronics and fundamentals on QED, SED, Molecular electronics and spintronics along with computational tools for modeling and simulation of nanoelectronics devices.

UNIT – I

Introduction to Nanoelectronics: Limitations of the conventional MOSFETs at Nanoscales, MOSFET Scaling & implications, Introductory concepts of Ballistic transport and Quantum confinement, Differences in Few Electron Devices (as analog version) and Single Electron Devices (as digital version) of Nanoelectronic devices

Nanostructures and Quantum Electronic Devices: Low-dimensional structures- Quantum wells, Quantum wires and Quantum dots; Density of states in low-dimensional structures; Quantum Interference Devices; Split –Gate Transistor; Electron – Wave Transistor; Resonant tunneling phenomena and its applications in diodes and transistors

09 Hrs

UNIT – II

Molecular Electronic: Overview & Basics; Fabrication of molecular electronics-based transistor devices; Conductivity of organic polymers- Conduction mechanism in organic polymers; Polymer Electronics; Self-Assembling Circuit.

08 Hrs

UNIT – III

Single Electron Devices: Principle of operation- Single-Electron Effect, Coulomb Blockade Phenomenon: Theoretical Quantum Dot Transistor - Energy of Quantum Dot system, Single-Electron Quantum-Dot Transistor, Single transistors; Conductance Oscillation and Potential Fluctuation; Transport under Finite temperature and Finite Bias; Coulomb Blockade Devices.

08 Hrs

UNIT – IV

Carbon Nanoelectronics: Carbon nanotubes - SWCNTs and MWCNTs; 1D quantization in nanotubes- van Hove singularities; Fabrication of CNTs; CNT FETs- Device characteristics, CNT-TUBFET, CNT-SET; and NanoWire FETs; Electronic structure of grapheme: FETs-GNRFETs.

08 Hrs

UNIT – V

Spintronics: Fundamentals of spintronics: Spintronic devices- spin diodes and spin transistors

Current Nanoelectronic Devices: Quantum Effects in MOSFETs, Strained Silicon, Fully Depleted SOI-MOSFET, Double-Gate MOSFET, Multi-gate MOSFETs, FIN-FET, Electrically Induced Junctions for EJ-MOSFETs, Ballistic Transport, Conductance Quantization, Quantum Point Contact Devices. **09 Hrs**

Text Books:

1	Shunri Oda, David Ferry	Nanoscale Silicon Devices, CRC Press, Taylor & Francis Group, 2015.
2	K. Goser, P. Glosekotter	Nanoelectronics and Nanosystems, Springer, 2005

Reference Books:

1	Suprio Datta	Lessons from nanoelectronics, World Scientific publisher, 2nd Edition, 2018
2	Karl Goser, Peter Glosekotter, Jan Dienstuhl	Nanoelectronics and Nanosystems- From Transistors to Molecular and Quantum Devices, Springer-Verlag 2004.
3	Supriyo Datta	Quantum Transport-From Atom to Transistor, Cambridge University press, 2012.

Course Outcomes: Students will be able to

CO1: Explain the concepts of ballistic transport and quantum confinement.

CO2: Describe the various nanostructures and its applications towards Quantum Electronic Devices.

CO3: Discuss the fundamentals of Molecular Electronics

CO4: Describe the fundamentals of Single Electron Devices and carbon based nanoelectronic devices.

CO5: Explain the fundamentals of Spintronics.

Design of CMOS Phase Locked Loops

Contact Hours/ Week	: 3+0+0(L+P+T)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours	: 00	SEE Marks :	50
Course Code	: S2LVSE34	Course Type:	PEC

Course Objective: To impart the knowledge of designing phase locked loops, Delay locked loops.

UNIT-I

Introduction: Introduction to Phase locked loops (PLLs), Basic operation of PLL and DLL architectures. Steady state analysis of basic PLL architectures.

09 Hrs

UNIT-II

Designing PFD and Charge pump: Phase detectors, Phase frequency detectors, Charge pump, Loop filters, Introduction to Charge pump based PLLs, Design methodology of charge pump based PLLs.

08 Hrs

UNIT-III

Oscillators: Basic principles, Cross coupled oscillators, Voltage controlled oscillators, VCOs with wide tuning range, Basic concepts, of phase noise.
Inverter based Ring oscillators, Basic differential ring oscillators.

08 Hrs

UNIT-IV

Frequency synthesis: Introduction to frequency synthesis, Basic Integer N – Synthesizer, Divider design: Pulse swallow divider, Dual modulus divider, Divider logic styles. Fractional N – Synthesizer: Basic concepts, Fractional divider using Delta sigma modulation technique.

08 Hrs

UNIT-V

Digital PLL (DPLL): Basic architecture of DPLL, Basic operation of Time to Digital conversion (TDC), Vernier TDC, Digitally controlled oscillator. Basics of Digital filters.
Clock and Data recovery circuits: Basic idea of clock and data recovery circuits, Bang-Bang Phase detector, Alexander phase detector, Hogge Phase detector.

09 Hrs

Text Books:

1	Behzad Razavi	Design of CMOS Phase locked loops, from circuit level to Architecture level, Cambridge university press, 2020.
2	Behzad Razavi	RF microelectronics, 2nd Edition Pearson education 2012

Reference Books:

1	F. Gardner	Phaselock Techniques, John Wiley & Sons, 2005.
2	R. Best	Phase-Locked Loops : Design, Simulation, and Applications, McGraw Hill, 2007.

Course Outcomes: students will be able to

CO1: Analyze PLL architecture.

CO2: Analyze and design PFDs and Charge pumps

CO3: Analyze and design VCOs and Ring oscillators.

CO4: Analyze and design dual modulus, integer -N and fractional dividers, Charge pump based Integer N and fractional PLLs.

CO5: Discuss the basics of Digital PLLs and Clock and data recovery circuits.

Hardware Security Systems

Contact Hours/ Week	: 3+0+0(L+P+T)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours	: 00	SEE Marks :	50
Course Code	: S2LVSE35	Course Type:	PEC

Course Objectives: To impart the knowledge on Hardware security and its implementation.

UNIT- I

Introduction: Introduction to modern cryptography and hardware security, Symmetric Key and Assymetric key cryptography, Historical ciphers, Perfect security and its limitations. Pseudo random number generators (PRGs), Secure and practical instantiation of PRGs.

08 Hrs

UNIT- II

Cryptanalysis: Introduction to Crypto analysis, Block ciphers, Inner structure of block ciphers, The advanced encryption standard (AES), Key scheduling in AES, Quantum safe cryptography, Field isomorphisms.

Hardware design of AES: Algorithm and architectural optimizations for AES Design, Circuit for the AES s-box, Implementation of the mixcolumns transformation. Compact AES s-box, Compact AES s-box on a normal basis.

09 Hrs

UNIT- III

Finite Field Arithmetic: Finite Field architectures, Hardware design and architecture for Finite field inverse.

Elliptic curve cryptography (ECC): Introduction ECC, Elliptic curve cryptoprocessor (ECCP). Point arithmetic on the ECCP, The Finite state machine of ECCP, Pipelining strategies for the scalar multiplier,

09 Hrs

UNIT- IV

Side Channel Analysis: Introduction to side channel analysis, Types of side channel attacks, Difference between Side channel analysis and Conventional Cryptanalysis

Power Analysis: Introduction to power analysis, power attacks, differential power attacks, Power counter measures,

08 Hrs

UNIT- V

Fault Analysis: Fault analysis of Crypto systems, Improved differential fault analysis (DFA) of AES, Multibyte and key scheduling based fault analysis of AES, Redundancy based fault intensity.

Micro architectural attacks: Cache timing attacks on block ciphers, Branch prediction attacks, Row hammer attacks.

Public key cryptosystem: RSA public key cryptosystem, Hybrid public key cryptosystem.

08 Hrs

Text Books:

1	Debdeep Mukhopadhyay, Rajat Subhra chakraborty	Hardware Security, Design, threats and safeguards, CRC press, 2015
2	Roger R. Dube	Hardware-Based Computer Security Techniques to Defeat Hackers - From Biometrics to Quantum Cryptography, John Wiley & Sons Inc; 1st edition (12 September 2008)

Course outcomes: At the end of the course the student will be able to:

CO1. Discuss about modern cryptography techniques.

CO2. Discuss advanced encryption standard (AES), analyze and Design \ AES circuits.

CO3. Discuss elliptic curve cryptography (ECC), analyze and design elliptic curve cryptoprocessors (ECCP).

CO4. Discuss about attacks related to side channel and power analysis.

CO5. Discuss about fault analysis, microarchitectural attacks and public key cryptosystem.

Professional Elective – IV

System on Chip Design

Contact Hours/ Week	:3+0+0(L+P+SDA)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total SDA Hours	: 00	SEE Marks :	50
Sub. Code	: S2LVSE41	Course Type:	PEC

Course Objective (CO): Enable students to learn the System on Chip design with different approaches and understand the concepts of embedded memories and network on chip topologies.

UNIT- I

Motivation for SoC Design - Review of Moore's law, benefits of system-on-chip integration in terms of cost, power, and performance. Typical goals in SoC design – cost reduction, power reduction, design effort reduction, performance maximization. Productivity gap issues and the ways to improve the gap. Comparison on System-on-Board, System-on-Chip, and System-in-Package

System On Chip Design Process: Canonical SoC Design, System Design flow - waterfall design flow, Spiral design flow, Top-down vs Bottom up design flows and Construct by Correction.

09 Hrs

UNIT- II

System level design issues

Specification requirement, Types of Specification. Standard Model: - Soft IP vs Hard IP. Role of Full-Custom Design in Reuse. Design for Timing Closure: Logic Design Issues and Physical Design Issues. Design for Verification: Verification Strategy. System Interconnect and On-Chip Buses. Design for Bring-Up and Debug. Design for Low Power. Design for Test: Manufacturing Test Strategies. Prerequisites for Reuse

08 Hrs

UNIT- III

Macro Design Process: Overview of IP Design, Key Features, Planning and Specifications, Macro design and Verification. Developing Hard Macros: Overview, Design Issues for Hard Macros, Hard Macro Design Process, Productization of Hard Macros.

08 Hrs

UNIT- IV

SoC Verification: -Verification technology options, Verification methodology, Verification languages, Verification IP Reuse, approaches. Verification and Device Test, Verification Plans. UVM overview, VLSI Packaging: Introduction, Packaging, Power Distribution, Input/Output, Chip-Package Co-design.

08 Hrs

UNIT- V

Embedded Memories –cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence. MESI protocol and Directory-based coherence.

Interconnect architectures for SoC: Bus architecture and its limitations. Network on Chip (NoC) topologies. Mesh-based NoC. Routing in an NoC. Packet switching and wormhole routing.

MPSoCs: Introduction to MPSoCs, Techniques for designing MPSoCs.

09 Hrs

Text Books:

1	Sudeep Pasricha and NikilDutt	On-Chip Communication Architectures: System on Chip Interconnect, Morgan Kaufmann Publishers, 2008
2	Rao R. Tummala, MadhavanSwaminathan	Introduction to system on package sop- Miniaturization of the Entire System, McGraw-Hill, 1st Edition, 2008.
3	Michael Keating, Pierre Bricaud	Reuse Methodology Manual for System on Chip designs , Kluwer Academic Publishers, 2nd edition, 2008

Course Outcomes: Students will be able to

CO1: Describe the benefits and different design process of SoC.

CO2: Discuss System-Level Design Issues, Rules and Tools.

CO3: Identify and select an appropriate macro design style for SOC design

CO4: Analyze the various methods of SOC verification issues and packaging techniques.

CO5: Analyze cache protocols, NOC topology and describe the design concepts of different types of MPSoCs.

CO6: Design selected circuit for a particular application using appropriate tool. Prepare the report.

System Verilog

Contact Hours/ Week	: 3+0+0(L+P+SDA)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total SDA Hours	: 00	SEE Marks :	50
Course Code	: S2LVSE42	Course Type:	PEC

Course Objectives: To impart the knowledge on system Verilog language to design, assertion and verify functionality of the system.

UNIT- I

Basics of Verification: Difference between ASIC verification and ASIC testing, Verification basics, Test benches, Layered Organization of Test benches. Importance of hardware verification languages and methodologies. **System Verilog data types and typedefs:** System Verilog data types, enhanced literal numbers syntax, 4-state and 2-state types, typedefs, enum, struct data type, Type parameters, $unit and $root. Packages, strings, static and dynamic type casting, Random number generation.

09 Hrs

UNIT- II

System Verilog operators, loops, jumps, functions: loops and jumps in system verilog, introduction to different always blocks, system verilog enhancements to tasks and functions, system verilog priority and unique modifiers for case and if statements, ‘time scale, system verilog time unit and time precision.

Structs, Unions, Packed and Unpacked Arrays, Semaphores and Mailboxes: Structs and its assignments, packed and unpacked arrays, array indexing, structs and packed structs, Unions and packed unions, dynamic arrays and methods, for each loop, associative arrays and methods, queues and concatenation operations, queue methods, semaphores and methods, Mail boxes and methods, bounded and unbounded mail boxes.

08 Hrs

UNIT- III

Class and Randomization: System verilog class basics, class declaration, class members and methods, class handles, class object construction, super and this keywords, object handles, user defined constructors, class extension and inheritance, chaining new() constructors, overriding class methods, extending class methods, local and protected keywords, constrained random variables, directed vs random testing, r and c class data types, randomize-randomizing class variables, random case, built-in-randomization methods, random sequence and examples. Randomization constraints, simple and multi-statement constraints.

08 Hrs

UNIT- IV

Interfaces: Interface overview, generic interfaces, interfaces vs records, how interfaces work, requirements of good interface, interface constructs, interface mode ports.

Program block: Fundamental test bench construction, program blocks, program block interaction with modules, final blocks, Test-bench stimulus/Verification vector timing strategies.
Clocking: Clocking blocks, clocking skews, clocking block scheduling, fork-join processes.

08 Hrs

UNIT- V

Constrained Random variables, Coverage, Methods and interfaces: Constraint distribution and set membership, constraint distribution operators, external constraints, covergroups, coverpoints, coverpoint bins and labels, cross coverage, covergroup options, coverage capabilities. Virtual class, why to use virtual class, virtual class methods and restrictions, polymorphism using virtual methods, pure virtual methods, pureconstraints, passing type parameters, virtual interfaces.
Assertions, Immediate and concurrent assertion, assertion operators and methods, assertion property and sequence.

09 Hrs

Text Books:

1	Christian B Spear	“SystemVerilog for Verification: A guide to learning the Testbench language features”, Springer publications, 3 rd edition, 2010.
2	VijayaRaghavan	“SystemVerilog Assertions”, Springer publications, 2005
3	Sutherland	“Systemverilog for Design”, Springer publications, 2006

Course Outcomes: Students will be able to
CO1: Identify and use appropriate data types for system Verilog programming.
CO2: Select and apply appropriate program constructs for System design.
CO3: Select and apply appropriate methods to write test benches.
CO4: Identify, select and apply different clocking schemes for optimization of designs.
CO5: Discuss constrained Random variables, Coverage, Methods and interfaces

RISC-V Processor Design

Contact Hours/ Week	: 3+0+0(L+P+T)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total Tutorial Hours	: 00	SEE Marks :	50
Course Code	: S2LVSE43	Course Type:	PEC

Course Objective: To impart the knowledge of RISC-V Instruction Set Architecture and its design.

UNIT- I

Evolution of the RISC-V Architecture: RISC-V Base Instruction Sets and Extensions. Comparison of RISC-V, MIPS, ARM and x86 Architectures, Programmers model for RV32I, Operation and addressing modes of Data Processing instructions, Control transfer instructions, Conditional branches, Assembly level programming examples.

09 Hrs

UNIT- II

Data Transfer Instructions, Control and Status Register Instructions, Pseudo Instructions, Assembler directives, RISC-V Machine level instruction formats: Base Instruction formats for R, I, S/B, U/J type instructions, immediate encodings. RISC-V memory map, Compiling, Assembling, Linking and Loading RISC-V programs, Exception handlers. Assembly level programming examples.

08 Hrs

UNIT- III

RISC-V Microarchitecture design: Architectural state and Instruction set, Design process, Performance analysis, Single cycle processor design: Single cycle data-path and control. Multi-cycle processor design: Multi-cycle data-path and control. Pipelined processor design:

08 Hrs

UNIT- IV

HDL representation of Single cycle processor: Controller, Main decoder, ALU decoder, Resettable flip-flop with enable, Data path, Extend unit, Multiplexers, Test bench, Top level module, Instruction memory and data memory.

08 Hrs

UNIT- V

Pipelined processor data-path and control. Hazards, Branch predictions, Superscalar processors, out-of-order processors, register renaming, Multithreading, Multiprocessors.

09 Hrs

Text Books:

1	Sarah L Harris David Money Harris	Digital Design and Computer Architecture RISC-V Edition, Morgan Kaufmann Publishers, 2022.
2	David Patterson, Andrew Waterman	RISC-V Reader: An Open Architecture Atlas, Strawberry Canyon, 1st Edition, 2017

Reference Books:

1	David A. Patterson John L. Hennessy	Computer Organization and Design The Hardware/Software Interface RISC-V Edition, Morgan Kaufmann Publishers, 2020
2	Edson Borin	Introduction to Assembly programming with RISC-V, 1st Edition, 2024, ISBN:978-65-00-15811-3
3	Anthony J Dos Reis	RISC-V Assembly Language, 2019 ISBN-13 : 978-1088462003

Course outcomes: On successful completion of this course, students will be able to:

CO1: Develop Assembly level programs for basic arithmetic and logical operations using RISC-V processor.
CO2: Interpret Assembly level instructions of RISC-V in to its Machine level code.
CO3: Design RISC-V Microarchitectures.
CO4: Develop HDL for different elements of RISC-V design.
CO5: Design pipelined RISC-V processor architecture.

Static Timing Analysis

Contact Hours/ Week	: 3+0+0(L+P+SDA)	Credits :	3.0
Total Lecture Hours	: 42	CIE Marks :	50
Total SDA Hours	: 00	SEE Marks :	50
Course Code	: S2LVSE44	Course Type:	PEC

Course Objectives: To impart the knowledge on static timing analysis in Digital IC design.

UNIT- I

Introduction: VLSI Physical Design flow, FPGA Design Flow, Introduction to static timing analysis (STA), STA at different design phases, Limitations of STA, Standard cells, Modeling of CMOS cells, Switching waveform, Propagation delay, Slew of a waveform, Skew between signals, Timing Arcs and Unateness, Min and Max Timing Paths,Clock Domains, Operating Conditions.

08 Hrs

UNIT- II

Standard Cell Library: Pin Capacitance, Timing modeling, Timing models for combinational cells and sequential cells, State dependent models, Power dissipation modeling, Cell library attributes: Area Specification, Function Specification, SDF Condition. Characterization and Operating Conditions.

08 Hrs

UNIT- III

Interconnect Parasitics: RLC for Interconnect, Wireload Models, Interconnect Trees, Specifying Wireload Models, Representation ofExtracted Parasitics, Detailed Standard Parasitic Format, Reduced Standard Parasitic Format, Standard Parasitic ExchangeFormat, Representing Coupling Capacitances, HierarchicalMethodology, Block Replicated in Layout, Reducing Parasitics forCritical Nets, Reducing Interconnect Resistance, Increasing WireSpacing, Parasitics for Correlated Nets.Delay Calculation Basics, DelayCalculation with Interconnect, Pre-layout Timing, Post-layoutTiming, Cell Delay using Effective Capacitance, InterconnectDelay, Elmore Delay, Higher Order Interconnect DelayEstimation, Full Chip Delay Calculation, Slew Merging, DifferentSlew Thresholds, Different Voltage Domains, Path DelayCalculation, Combinational Path Delay, Path to a Flip-flop, Inputto Flip-flop Path, Flip-flop to Flip-flop Path, Multiple Paths, SlackCalculation.

09 Hrs

UNIT- IV

Configuring the STA Environment: STA Environment, Specifying Clocks, Clock Uncertainty, Clock Latency, GeneratedClocks, Example of Master Clock at Clock Gating Cell Output, Generated Clock using Edge and Edge_shift Options, GeneratedClock using Invert Option, Clock Latency for Generated Clocks, Typical Clock Generation Scenario, Constraining Input Paths, Constraining Output Paths, Example A, Example B, Example C,Timing Path Groups, Modeling of External Attributes, ModelingDrive Strengths, Modeling Capacitive Load, Design Rule Checks, Virtual Clocks, Refining the Timing Analysis, Specifying Inactive

Signals, Breaking Timing Arcs in Cells, Point-to-Point Specification, Path Segmentation

08 Hrs

UNIT- V

Timing Verification: Setup Timing Check, Flip-flop to Flip-flop Path, Input to Flip-flop Path, Input Path with Actual Clock, Flip Flop To Output Path, Input to Output Path, Frequency Histogram,Hold Timing Check, Flip-flop to Flip-flop Path, Hold Slack Calculation, Input to Flip-flop Path, Flip-flop to Output Path,Flip-flop to Output Path with Actual Clock, Input to Output Path,vMulticycle Paths, Crossing Clock Domains, False Paths, Half- Cycle Paths, Removal Timing Check, Recovery Timing Check,Timing across Clock Domains, Slow to Fast Clock Domains, Fast To Slow Clock Domains, Half-cycle Path - Case 1, Half-cycle Path -Case 2, Fast to Slow Clock Domain, Slow to Fast Clock Domain,Multiple Clocks, Integer Multiples, Non-Integer Multiples, Phase Shifted.

09 Hrs

Text Books:

1	J. Bhasker, R Chadha	Static Timing Analysis for Nanometer Designs: A Practical Approach, Springer 2009
2	Sridhar Gangadharan, Sanjay Churiwala	Constraining Designs for Synthesis and Timing Analysis – A Practical Guide to Synopsis Design Constraints (SDC), Springer 2013
3	Giovanni De Micheli	Synthesis and Optimization of Digital Circuits, TMH, 1994

Course outcomes: At the end of the course the student will be able to:

CO1. Evaluate the delay of any given digital circuits.

CO2. Prepare the resources to perform the static timing analysis using EDA tool.

CO3. Prepare timing constraints for the design based on the specification.

CO4. Generate the timing analysis report using EDA tool for different checks.

CO5. Perform verification and analyse the generated report to identify critical issues and bottleneck for the violation and suggest the techniques to make the design to meet timing

VLSI Design Lab

Lab work Hours/Week	: 0+4+0 (L+P+T)	Credits :	2.0
Total Lecture Hours	: 00	CIE Marks :	50
Total Lab Hours	: 56	SEE Marks :	50
Course Code	: S2LVSL1	Course Type:	PCCL

Course Objective: Analyse, Design and simulate digital and analog MOSFET circuits for various applications.

List of Experiments:

1. Design a given logical operation using CMOS design style.

a. Draw the schematic and verify the design parameters with the help of
   i. Transient Analysis to verify the truth table

b. Draw the Layout and verify the DRC.

c. Extract RC and back annotate the same and verify the Design

2. Design a CMOS full adder for given specifications.

a. Draw the schematic and verify the design parameters with the help of
   i. Transient Analysis to verify the truth table

b. Draw the Layout and verify the DRC.

c. Extract RC and back annotate the same and verify the Design

3. Design a Common Source amplifier with resistive load for given specifications.

a. Draw the schematic and verify the design parameters with the help of
   i. DC Analysis (Calculate the theoretical value for Av)
   ii. Transient Analysis (Verify theoretical value of Av with its Practical value).

b. Draw the Layout and verify the DRC, LVS

c. Extract RC and back annotate the same and verify the Design

4. Design a Common Source amplifier with Active load using Current mirror for given specifications.

Complete the design flow mentioned below:

a. Draw the schematic and verify the design parameters with the help of
   i. DC Analysis (Calculate the theoretical value for Av)
   ii. Transient Analysis (Verify theoretical value of Av with its Practical value).

b. Draw the Layout and verify the DRC, LVS

c. Extract RC and back annotate the same and verify the Design

5. Design a Common drain amplifier with Active load for given specifications.

Complete the design flow mentioned below:

a. Draw the schematic and verify the design parameters with the help of
   i. DC Analysis (Calculate the theoretical value for Av)
   ii. Transient Analysis (Verify theoretical value of Av with its Practical value).

b. Draw the Layout and verify the DRC, LVS

c. Extract RC and back annotate the same and verify the Design
6. Design a Differential Amplifier with Active load using Current mirror for given specifications.

Complete the design flow mentioned below:

a. Draw the schematic and verify the design parameters with the help of
   i. DC Analysis (Calculate the theoretical value for Av)
   ii. Transient Analysis (Verify theoretical value of Av with its Practical value).
b. Draw the Layout and verify the DRC, LVS.
c. Extract RC and back annotate the same and verify the Design.

7. Design a Operational Amplifier with Active load using Current mirror for given specifications.

Complete the design flow mentioned below:

a. Draw the schematic and verify the design parameters with the help of
   i. DC Analysis
   ii. Transient Analysis
b. Draw the Layout and verify the DRC, LVS
c. Extract RC and back annotate the same and verify the design

8. Design a 4 bit binary weighted DAC / 4-bit R-2R Ladder DAC for given specifications.

Complete the design flow mentioned below:

a. Draw the schematic and verify the design parameters with the help of
   i. DC Analysis
   ii. Transient Analysis
b. Draw the Layout and verify the DRC, LVS
c. Extract RC and back annotate the same and verify the design

Course Outcomes: Student will be able to

CO1: Analyze and Design analog circuits and simulate using EDA tool and prepare the report.

CO2: Analyze and Design digital circuits and simulate using EDA tool and prepare the report.

Ability / Skill Enhancement Courses

Peripheral and IO Firmware development

Contact Hours/ Week	: 0+2+0(L+P+SDA)	Credits :	1.0
Total Lecture Hours	: 00	CIE Marks :	50
Total Practical Hours	: 28	SEE Marks :	50
Course Code	: S2LVSA201	Course Type:	AEC

Course Objectives: To impart the knowledge on Peripheral and IO Firmware development using embedded C.

1. Develop firmware delay routines for generating delays in ms, us, and seconds using Timer module.
2. Develop firmware to generate PWM signal given pulse width and period of the signal.
3. Develop firmware to UART module for transferring and receiving a given string of data with string size as inputs or null character as the end of the string.
4. Develop firmware for SPI module to transmit and receive data.
5. Develop firmware for the I2C module to transmit the data.
6. Develop firmware for the I2C module to receive the data.
7. Develop firmware to display the given image and data on Graphic LCD.

Course outcomes: At the end of the course the student will be able to:

CO1. Design and develop Firmware for different peripherals and IOs.

CO2. Design and develop test circuits for testing the firmwares of different peripherals and IOs.

Machine Learning for Embedded Systems

Contact Hours/ Week	: 0+2+0(L+P+SDA)	Credits :	1.0
Total Lecture Hours	: 00	CIE Marks :	50
Total Practical Hours	: 28	SEE Marks :	50
Course Code	: S2LVSA202	Course Type:	AEC

1: Introduction to Machine Learning for Embedded Systems
- Lab: Set up Python, Jupyter Notebook, and required ML libraries (TensorFlow) on the desktop.

2: Fundamentals of Machine Learning and Deep Learning
- Lab: Explore the MNIST dataset, visualize data, and preprocess it (normalization, reshaping).

3: Building a Simple Neural Network Model
- Lab: Build and train a basic neural network for digit recognition using MNIST.

4: Evaluation and Optimization of the Model
- Lab: Evaluate the trained model on test data; tune hyperparameters to improve accuracy.

5: Introduction to Convolutional Neural Networks (CNNs)
- Lab: Modify the previous model to a CNN architecture and train it on MNIST.

6: Training and Testing the CNN Model
- Lab: Train the CNN model on MNIST and test its performance; implement dropout for regularization.

7: Introduction to Model Compression and Optimization
- Lab: Apply quantization to the CNN model for reduced size and faster inference.

8: Conversion to TensorFlow Lite for Deployment
- Lab: Convert the trained CNN model to TensorFlow Lite format.

9: Introduction to the Raspberry Pi for ML Applications
- Lab: Set up the Raspberry Pi, install Python, and configure TensorFlow Lite.

10: Model Deployment on Raspberry Pi
- Lab: Transfer the TensorFlow Lite model to Raspberry Pi and perform initial tests.

11: Testing and Validating Model Performance on Raspberry Pi
- Lab: Measure inference latency and memory usage on Raspberry Pi using sample images.

12: Real-Time Application Development and Final Testing
- Lab: Connect a camera module to Raspberry Pi and deploy a real-time digit recognition application.

13: Final Project Review and Presentation
- Lab: Final project demonstration; students present their digit recognition system and deployment process.

Data Analytics Using R-Programming

Contact Hours/ Week	: 0+2+0(L+P+SDA)	Credits :	1.0
Total Lecture Hours	: 00	CIE Marks :	50
Total Practical Hours	: 28	SEE Marks :	50
Course Code	: S2LVSA203	Course Type:	AEC

Course objectives:
This course will enable students to:

1.	Learn R Programming language.
2.	Learn Data visualization.
3.	Analyze data sets using R

List of Experiments:

1.	Introduction to R Programming.
2.	Data Visualisation and Manipulation in R
3.	Reading Data from files
4.	Data Visualization using Tables, charts and plots.
5.	Visualising Measures of Central Tendency, Variation, and Shape.
6.	Data visualisation using Box plots, Pareto diagrams
7.	Find the mean median standard deviation and quantiles of a set of observations.
8.	Generate and Visualize Discrete and continuous distributions using the statistical environment

TEXT BOOKS

1	Maria Dolores Ugarte , Ana F. Militino , Alan T. Arnholt.	Probability and Statistics with R, 2nd Edition on, CRC Press, 2016.
2.	P. Dalgaard. Introductory Statistics with R	2nd Edition. (Springer 2008). (eBook).

REFERENCE BOOKS

1.	" Probability & Statistics with R for Engineers and Scientists”, 2nd Edition on, CRC Press, 2016.	" Probability & Statistics with R for Engineers and Scientists”, 2nd Edition on, CRC Press, 2016.

Course Outcomes:
Upon completion of this course the student will be able to:

CO1	Develop programs using R-data types, objects and frames.
CO2	Perform data analysis and visualization using R-programming.

SIDDAGANGA INSTITUTE OF TECHNOLOGY, TUMAKURU-03
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SCHEME OF TEACHING AND EXAMINATION

III SEMESTER M.Tech. VLSI Design and Embedded Systems

For the students who are willing to take up a two-semester duration Industry/Research Internship Leading to Project work /start-up

IIISEMESTER (A)

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week			Examination				Credits
				Theory	Practical/ Mini–Project/ Internship	Tutorial/ Skill Development Activities	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	P	SDA					
1	PEC/ MDC	S3LVS301/401	(Online Courses) 12 weeks duration							100	3
2		S3LVS302/402	(Online Courses)12 weeks duration							100	3
		S3LVS303/403	(Online Courses)12 weeks duration							100	3
3	INT	S3LVSINT	Research Internship /Industry-Internship leading to project work/ Startup	Two-semester duration, SEE in the IV semester which leads to project work /start-up			03	**100**	- - -	100	3
TOTAL							**03**	**100**	**-**	**400**	**12**

S3LVS30x/40x	**(Online Courses) 12 weeks duration**
S3LVS301/401	Digital VLSI Testing
S3LVS302/402	VLSI Design flow RTL to GDS
S3LVS303/403	Introduction to Industry 4.0 and Industrial Internet of Things
S3LVS304/404	Computer Architecture
S3LVS305/405	Multi core Computer Architecture
S3LVS306/406	C-based VLSI Design
S3LVS307/407	Fundamentals of Micro and Nanofabrication
S3LVS308/408	Introduction to Virtual Reality
S3LVS309/409	Sensors and Actuators
S3LVS310/410	Thin film Technology
S3LVS311/411	Fundamentals of Micro and Nanofabrication
S3LVS312/412	Sensor Technologies, Physics, fabrication and circuits

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SCHEME OF TEACHING AND EXAMINATION
IV SEMESTER M.Tech. VLSI Design and Embedded Systems

IV SEMESTER (A)

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work	Duration in hours	CIE Marks	SEE Marks Viva voce	Total Marks	
				L	P					
1	INT	S4INT401	Research Internship / Industry Internship Leading to Project Work/Start-up	Two Semester Duration		03	100	100	200	12
2	PROJ	SPROJ402	Project			03	100	100	200	16
			TOTAL			06	200	200	400	28

INT: Industry/ Research Internship leading to the project work /startup **PROJ:** Project work outcome of Internship (Project Phase-II is Viva voce SEE) Taking up a two-semester Industry/Research Internship that leads to project work or a start-up can be a highly rewarding experience for students. It allows them to apply theoretical knowledge in practical settings, gain valuable industry or research experience, and potentially develop innovative solutions or business ideas. Here are some key steps and considerations for students pursuing such an internship:Industry Internship: The main objective of the industry internship is to ensure that the intern is exposed to a real-world environment and gain practical experience. Often, it may be a practical exposure to the theory that has been learned during the academic period. The industry internship helps students understand of analytical concepts and tools, hone their skills in real-life situations, and build confidence in applying the skills learned.

Research Internship: A research internship is an opportunity for students or early career professionals to gain hands-on experience in conducting research under the guidance of a mentor or within a research team. These internships can take place in academic institutions, research organizations, government agencies, or private companies

Research /Industry Internship: In the third-semester Students have to be in touch with a guide/mentor/coordinator and regularly submit the report referred to the progress internship. Based on the progress report the Guide/Mentor/coordinator has to enter the CIE marks at the end of the 3rd semester. At the beginning of the 4th semester, students have to define the project topic out of the learning due to the Internship, upon completion of the project work he/she has to attend the SEE at the parent Institute.

Internship Leading to Start-up: An internship that leads to a startup is an exciting pathway, blending real-world experience with entrepreneurial ambition. Here's a comprehensive guide to transitioning an internship experience into launching your startup: 1) Maximize your internship experience, 2) Identifying Viable Business Ideas, 3) Research and Validation 4) Building a Business Plan 5) Networking and Mentorship 6) Securing Funding 7) Establishing Startup 8) Launching and Marketing. By following these steps, you can effectively transition from an internship to launching a successful startup. This journey requires dedication, resilience, and a willingness to learn and adapt.

Mxxx301/401 to 303/403: MOOC courses of 12 weeks duration are the courses suggested by the Board of Studies of the University and will be displayed on www.online.vtu.ac.in. The online courses selected should not be the same as those studied in the first and second semesters of the program. The student will not be eligible to get their degree if they unintentionally select online courses that match previously finished courses. These courses are not considered for the vertical progression; however, qualifying for these courses and earning the credits is a must for the award of the degree. It is permitted to complete these online MOOC courses either in 3rd semester or in 4th semester.

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SCHEME OF TEACHING AND EXAMINATION

III SEMESTER M.Tech. VLSI Design and Embedded Systems

For the students who are willing to take an Industry Internship for one-semester duration and independent project work next semester											
III SEMESTER (B)											
				Teaching Hours /Week			**Examination**				
	Course	**Course Code**	**Course Title**	**Theory**	**Practical/ Mini– Project/ Internship**	**Tutorial/ Skill Development Activities**	**Duration in hours**	**CIE Marks**	**SEE Marks**	**Total Marks**	**Credits**
				L	P	SDA					
1		S3LVS301/401	(Online Course) (12 weeks courses)							**100**	**3**
	MDC/ PEC	S3LVS302/402	(Online Course) (12 weeks courses)							**100**	**3**
2		S3LVS303/403	(Online Courses) (12-week course)							**100**	**3**
3	INT	S3LVSINT	Industry Internship	One semester Duration			**03**	**100**	**100**	**200**	**11**
TOTAL				**00**	**00**	**00**	**03**	**100**	**100**	**500**	**20**

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SCHEME OF TEACHING AND EXAMINATION

IV SEMESTER M.Tech. VLSI Design and Embedded Systems

IV SEMESTER (B)										
	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work	Duration in hours	CIE Marks	SEE Marks Viva voce	Total Marks	
				L	P					
1	Project	S4LVSPR	Project work	--	08	03	100	100	200	20
TOTAL				**00**	**08**	**03**	**100**	**100**	**200**	**20**

Industry Internship: The main objective of the industry internship is to ensure that the intern is exposed to a real-world environment and gains practical experience. Often, it may be a practical exposure to the theory that has been learned during the academic period. The industry internship helps students understand of analytical concepts and tools, hone their skills in real-life situations, and build confidence in applying the skills learned. The students who take up a one-semester Internship in the Industry have to appear SEE at the institute at the end of the semester as per the examination calendar.

Project Work: Students in consultation with the guide shall carry out literature survey/ visit industries to finalize the topic of the Project. Subsequently, the students shall collect the material required for the selected project, prepare a synopsis, and narrate the methodology to carry out the project work. Each student, under the guidance of a Faculty, is required to

- Present the seminar on the selected project orally and/or through Power Point slides.
- Answer the queries and be involved in debate/discussion.
- Submit two copies of the typed report with a list of references.
- The participants shall take part in discussions to foster a friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident

CIE marks for the project report (20 marks), seminar (20 marks) and question and answer (10 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session by the student) by the committee constituted for the purpose by the Principal. The committee shall consist of internal guide and a faculty from the department with the senior most acting as the Chairperson.

Semester End Examination SEE marks for the project report (30 marks), seminar (10 marks) and question and answer session (10 marks) shall be awarded (based on the quality of the report and presentation skill, participation in the question and answer session) by the examiners appointed by the University.

Mxxx301/401 to 303/403: MOOC courses of 12 weeks duration are the courses suggested by the Board of Studies of the University and will be displayed on www.online.vtu.ac.in. The online courses selected should not be the same as those studied in the first and second semesters of the program. The student will not be eligible to get their degree if they unintentionally select online courses that match previously finished courses. These courses are not considered for the vertical progression;

However, qualifying for these courses and earning the credits is a must for the award of the degree. It is permitted to complete these online MOOC courses either in 3^{rd} semester or in 4^{th} semester.

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SCHEME OF TEACHING AND EXAMINATION
III SEMESTER M.Tech. VLSI Design and Embedded Systems

For the students who are willing to take a research-leading paper publication in Q1/Q2/Q3 Journals and to a PhD Registration											
III SEMESTER (C)											
	Course	**Course Code**	**Course Title**	**Teaching Hours /Week**			**Examination**				**Credits**
				Theory	**Practical/ Mini–Project/ Internship**	**Tutorial/ Skill Development Activities**	**Duration in hours**	**CIE Marks**	**SEE Marks**	**Total Marks**	
				L	P	SDA					
1	PCC/I PCC/ MDC/ PEC	S3LVS301/401	(Online Course) (12 weeks courses)							100	3
		S3LVS302/402	(Online Course) (12 weeks courses)							100	3
2		S3LVS303/403	(Online Courses) (12-week course)							100	3
		S3LVS304/404	(Online Courses) (12-week course)							100	3
3	PROJ	S3LVSPR	Project Phase-I	One semester Duration			03	100	-	100	6
TOTAL				**00**	**00**	**00**	**03**	**100**	-	**500**	**18**

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SCHEME OF TEACHING AND EXAMINATION
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IV SEMESTER (C)												
Sl. No	Course	Course Code		Course Title	Teaching Hours /Week		Examination					Credits
					Theory	Practical/ Field work	Duration in hours	CIE Marks	SEE Marks Viva voce	Total Marks		
					L	P						
1	Project	S4LVSPR		Project work	--	08	03	100	100	200		22
TOTAL					00	08	03	100	100	200		22

The research section of the university has to announce the number of seats for M.Tech. students who are seeking PhD (research study) admission through a project leading to the publication of the paper in Q1/Q2/Q3 journals. Only full-time research work will be permitted in the university department or approved research centers of the affiliated colleges of the university (guidelines need to be set up).

Based on Seat availability, the students are permitted to register for project work leading to the publication of papers in Q1/Q2/Q3 journals and admission to research (PhD) in their 3rd semester of the M.Tech., program

Project Phase-1 Project Phase-I, typically the initial phase in any project, is crucial as it lays the foundation for the entire project. This phase involves defining the project's scope, objectives, and initial planning. Here's a structured approach to effectively carry out Project Phase-I:

Project Charter: Outlines the project's purpose, objectives, and stakeholders.
Scope Statement: Defines the project boundaries and deliverables.
Requirements Document: Captures all project requirements.
Project Plan: Details the approach, timeline, and resource allocation.
Risk Management Plan: Identifies and plans for potential risks.
Feasibility Study Report: Assesses technical, economic, and operational feasibility.

Students in consultation with the guide shall carry out literature survey/ visit industries to finalize the topic of the Project. Subsequently, the students shall collect the material required for the selected project, prepare a synopsis, and narrate the methodology to carry out the project work. Each student, under the guidance of a faculty, is required to Present the seminar on the selected project orally and/or through power point slides. Answer the queries and be involved in debate/discussion. Submit two copies of the typed report with a list of references.

The participants shall take part in discussions to foster a friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

Continuous Internal Evaluation (100 Marks).

CIE marks for the project report (60 marks), seminar (20 marks) and question and answer (20 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session by the student) by the committee constituted for the purpose by the Principal. The committee shall consist of an internal guide and a faculty from the department with the senior most acting as the Chairperson.

Project Work Phase - II: Each student shall be involved in carrying out the project work jointly in constant consultation with internal guide and external guide and prepare the project report as per the norms of the university to avoid plagiarism. Phase II of a project typically involves the detailed execution of the planned activities, continuous monitoring and control of the project's progress, and making necessary adjustments to ensure the project stays on track. Keep detailed records of all project activities, decisions, and changes. Ensure all project documentation is organized and accessible. Conduct a final project review to evaluate overall performance, achievements, and lessons learned. Document best practices and areas for improvement for future projects.

Paper Publication Process: Publishing a research paper based on your project in a Q1/Q2/Q3 journal involves several key steps, from writing the manuscript to navigating the peer review process. Here's a comprehensive guide:

Writing the Manuscript: Choose a clear and concise title that accurately reflects the content. Write an abstract summarizing the research question, methods, results, and conclusions.

Literature Review: Review relevant existing research to establish the foundation of your study. Identify gaps that your research aims to fill.

Methodology: Describe the research design, methods, and procedures in detail. Include information on data collection, analysis, and any tools or software used.

Results: Present the findings of your research clearly and logically. Use tables, figures, and charts to illustrate key results.

Discussion: Interpret the results and explain their implications. Compare your findings with existing research and discuss any discrepancies or new insights.

Conclusion: Summarize the main findings and their significance. Suggest potential future research directions.

References: Cite all sources used in your research following the journal's citation style.

Journal Selection: Choose a journal that aligns with the scope and focus of your research. Consider the journal's impact factor (Q1, Q2, Q3) and audience.

Review Journal Guidelines: Carefully read the journal's submission guidelines and ensure your manuscript adheres to them.

Prepare Your Manuscript: Format your manuscript according to the journal's guidelines. Include all required sections and supplementary materials.

Cover Letter: Write a cover letter to the journal editor highlighting the significance of your research and why it fits the journal.

Submit the Manuscript: Use the journal's online submission system to submit your manuscript. Ensure all required information and documents are included.

Semester End Examination SEE marks for the project report (60 marks), seminar (20 marks) and question and answer session (20 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session) by the examiners appointed by the University.