SIDDAGANGA INSTITUTE OF TECHNOLOGY,

TUMAKURU 572103, KARNATAKA, INDIA

DEPARTMENT OF ELECTRONICS AND INSTRUMENTATION ENGINEERING

SCHEME & SYLLABUS

OF

PG Course on

VLSI Design and Embedded Systems

2022-23

ACADEMIC YEAR: 2022-23

SIDDAGANGA INSTITUTE OF TECHNOLOGY, TUMAKURU-03

(An autonomous Institute under Visvesvaraya Technological University)

SCHEME OF TEACHING AND EXAMINATION

I SEMESTER M.Tech. VLSI Design and Embedded Systems

Sl. No.	Course Type and Course Code		Course Title	Teaching Hours per Week			Examination				Credits
				Theory L	Practical / Seminar P	Tutorial / Skill Development Activities T/SDA	Duration in hrs.	CIE Marks	SEE Marks	Total Marks	
1.	BSC	N1PGMAT	Mathematics Course specific to branch	3	0	0	3	50	50	100	3
2.	IPCC	N1LVS01	VLSI Design	3	2	0	3	50	50	100	4
3.	PCC	N1LVS02	Analog IC Design	3	0	2	3	50	50	100	4
4.	PCC	N1LVS03	ARM Microcontroller and its Applications	2	0	2	3	50	50	100	3
5.	PCC	N1LVS04	Digital System Design Using Verilog	2	0	2	3	50	50	100	3
6.	PEC	N1LVSE1x	Professional Elective – 1	2	-	2	3	50	50	100	3
7.	MCC	N1PGRM	Research Methodology and IPR	3	0	0	3	50	50	100	3
8.	PCCL	N1LVSL1	Embedded Systems Lab	1	2	0	3	50	50	100	2
9.	AUD/ AEC	N1LVSAUD / N1LVSAEC	BoS Recommended online course	Classes and Evaluation Procedures are as per the policy of the online course providers							0
Total				**19**	**4**	**8**		**500**	**400**	**900**	**25**

Professional Elective 1			
N1LVSE11	ASIC Design	N1LVSE13	VLSI for Digital Signal Processing
N1LVSE12	VLSI Design Automation	N1LVSE14	Nano Electronics

Note: **BSC**-Basic Science Courses, **IPCC**-Integrated Professional Core Courses, **PCC**: Professional Core Course, **PEC:** Professional Elective

Course, **MCC**- Mandatory Credit Course, **PCCL**-Professional Core Course Lab, **NCMC-**Non Credit Mandatory Course
AUD/AEC –Audit Course / Ability Enhancement Course(A pass in AUD/AEC is mandatory for the award of the degree)
L-Lecture, **P**-Practical, **T/SDA**-Tutorial / Skill Development Activities (Hours are for Interaction between faculty and students)

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with practical of the same course. The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper.

Audit Courses /Ability Enhancement Courses suggested by BoS (ONLINE courses):
Audit Courses are prerequisite courses suggested by the concerned Board of Studies.
Ability Enhancement Courses will be suggested by the BoS if prerequisite courses are not required for the programs.

- These courses are prescribed to help students to enhance their skills connected to the field of specialization as well allied fields that leads to employable skills. Involving in learning such courses are impetus to lifelong learning.
- The courses under this category are online courses published in advance and approved by the concerned Board of Studies.
- Registration to Audit /Ability Enhancement Course shall be done in consultation with the mentor and is compulsory during the concerned semester.
- In case a candidate fails to appear for the proctored examination or fails to pass the selected online course, he/she can register and appear for the same course if offered during the next session or register for a new course offered during that session, in consultation with the mentor.

The Audit / Ability Enhancement Course carries no credit and is not counted for vertical progression. However, a pass in such a course is mandatory for the award of the degree.

Skill development activities: in a concerned course, the students should

- Interact with industry (small, medium, and large).
- Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
- Involve in case studies and field visits/ fieldwork.
- Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
- Handle advanced instruments to enhance technical talent.
- Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
- Work on different software to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

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SCHEME OF TEACHING AND EXAMINATION

II SEMESTER M.Tech. VLSI Design and Embedded Systems

Sl. No.	Course Type and Course Code		Course Title	Teaching Hours per Week			Examination				Credits
				Theory	Practical / Seminar	Tutorial / Skill Development Activities	Duration in hrs.	CIE Marks	SEE Marks	Total Marks	
				L	P	T/SDA					
1.	IPCC	N2LVS01	Real time operating systems	3	2	0	3	50	50	100	4
2.	PCC	N2LVS02	VLSI Process Technology	3	0	2	3	50	50	100	4
3.	PCC	N2LVS03	Design of IoT Systems	2	0	2	3	50	50	100	3
4.	PEC	N2LVSE2x	Professional Elective – 2	2	0	2	3	50	50	100	3
5.	PEC	N2LVSE3x	Professional Elective – 3	2	0	2	3	50	50	100	3
6.	OEC	N2OExx	Open Elective	3	0	0	3	50	50	100	3
7.	MPS	N2LVSMPS	Mini Project with Seminar	0	4	2	--	100	--	100	3
8.	PCCL	N2LVSL1	VLSI Design Lab	1	2	0	3	50	50	100	2
9.	AEC	ARAS	Aptitude Related Analytical Skills	36 Hrs. for the entire semester			2	50	50	100	0
10	AUD/ AEC	N2LVSAUD / N2LVSAEC	BoS Recommended online course	Classes and Evaluation Procedures are as per the policy of the online course providers							0
	Total			**16**	**8**	**10**		**500**	**400**	**900**	**25**

Note: **IPCC**-Integrated Professional Core Courses, **PCC**: Professional Core Course, **PEC:** Professional Elective Course, **OEC**- Open Elective Course **MPS**- Mini Project with Seminar, **PCCL**-Professional Core Course Lab, **AUD/AEC** –Audit Course / Ability Enhancement Course (A pass in AUD/AEC is mandatory for the award of the degree) **L**-Lecture, **P**-Practical, **T/SDA**-Tutorial / Skill Development Activities (Hours are for Interaction between faculty and students)

Professional Elective 2		**Professional Elective 3**		**Open Elective 1**	
N2LVSE21	CMOS RF Circuit Design	N2LVSE31	System on Chip (SoC) Design	N2OE01	Embedded Systems
N2LVSE22	Mixed Signal Circuit Design	N2LVSE32	System Verilog	N2OE02	CMOS RF Circuit Design
N2LVSE23	VLSI Testing and Verification	N2LVSE33	Low power VLSI Design.		
N2LVSE24	Design of CMOS Phase Locked Loops	N2LVSE34	Wireless sensor network		
N2LVSE25	DSP Architecture	N2LVSE35	Interface and Noise control technique in Electronic System design		

1. **Mini Project with Seminar:** This may be hands-on practice, survey report, data collection and analysis, coding, mobile app development, field visit and report preparation, modelling of system, simulation, analysing and authenticating, case studies, etc.
   CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide, if any, and a senior faculty of the department. Students can present the seminar based on the completed mini-project. Participation in the seminar by all postgraduate students of the program shall be mandatory.
   The CIE marks awarded for Mini-Project work and Seminar, shall be based on the evaluation of Mini Project work and Report, Presentation skill and performance in Question and Answer session in the ratio 50:25:25. Mini-Project with Seminar shall be considered as a head of passing and shall be considered for vertical progression as well as for the award of degree. Those, who do not take-up/complete the Mini Project and Seminar shall be declared as fail in that course and have to complete the same during the subsequent semester. **There is no SEE for this course.**

2. Internship: All the students shall have to undergo a mandatory internship of **06 weeks** during the vacation of II and III semesters. A University examination shall be conducted during III semester and the prescribed internship credit shall be counted in the same semester. The internship shall be considered as a head of passing and shall be considered for vertical progression as well as for the award of degree. Those, who do not take-up/complete the internship shall be declared as fail in the internship course and have to complete the same during the subsequent University examination after satisfying the internship requirements.

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SCHEME OF TEACHING AND EXAMINATION

III SEMESTER M.Tech. VLSI Design and Embedded Systems

Sl. No.	Course Type and Course Code		Course Title	Teaching Hours per Week			Examination				Credits
				Theory	Practical / Seminar	Tutorial / Skill Development Activities	Duration in hrs.	CIE Marks	SEE Marks	Total Marks	
				L	P	T/SDA					
1.	PROJ	N3LVSPR	Project Work Phase – 1	0	6	0	--	100	--	100	3
2.	SP	N3LVSSP	Societal Project	0	6	0	--	100	--	100	3
3.	INT	N3LVSINT	Internship	(06 weeks Internship completed during the intervening vacation of II and III semesters)			3	50	50	100	6
	Total			0	12	0		250	50	300	12

Note: **PROJ**-Project Work Phase-1, **SP** –Societal Project, **INT-**Internship
L-Lecture, **P**-Practical, **T/SDA**-Tutorial / Skill Development Activities (Hours are for Interaction between faculty and students)

1. **Project Work Phase-1:** The project work shall be carried out individually. However, in case a disciplinary or interdisciplinary project requires more participants, then a group consisting of not more than three shall be permitted.
   Students in consultation with the guide/co-guide (if any) in disciplinary project or guides/co-guides (if any) of all departments in case of multidisciplinary projects, shall pursue a literature survey and complete the preliminary requirements of the selected Project work. Each student shall prepare a relevant introductory project document, and present a seminar.
   CIE marks shall be awarded by a committee comprising of HoD as Chairman, all Guide/s and co-guide/s (if any) and a senior faculty of the concerned departments. The CIE marks awarded for project work phase -1, shall be based on the evaluation of Project Report, Project Presentation skill, and performance in the Question and Answer session in the ratio of 50:25:25. **There is no SEE for this course**.
2. **Societal Project:** Students in consultation with the internal guide as well as with external guide (much preferable) shall involve in applying technology to workout/proposing viable solutions for societal problems.
   CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide if any, and a senior faculty of the department. The CIE marks awarded, shall be based on the evaluation of Project Report, Project Presentation skill, and performance in the Question and Answer session in the ratio of 50:25:25.
   Those, who have not pursued /completed the Societal Project, shall be declared as fail in the course and have to complete the same during subsequent semester/s after satisfying the Societal Project requirements. **There is no SEE for this course**.
3. **Internship:** Those, who have not pursued /completed the internship, shall be declared as fail in the internship course and have to complete the same during subsequent University examinations after satisfying the internship requirements. Internship SEE (University examination) shall be as per the University norms.
   CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide if any, and a senior faculty of the department. The CIE marks awarded for project work phase -1, shall be based on the evaluation of Project Report, Project Presentation skill, and performance in the Question and Answer session in the ratio of 50:25:25.

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SCHEME OF TEACHING AND EXAMINATION

IV SEMESTER M.Tech. VLSI Design and Embedded Systems

Sl. No.	Course Type and Course Code		Course Title	Teaching Hours per Week			Examination				Credits
				Theory	Practical / Field work	Tutorial / Skill Development Activities	Duration in hrs.	CIE Marks	SEE Marks	Total Marks	
				L	P	T/SDA					
1.	PROJ	N4LVSPR	Project Work Phase – 2	0	36	0	3	100	100	100	18
	Total			0	36	0		**100**	**100**	**100**	**18**

Note: **PROJ**-Project Work Phase-2, **L**-Lecture, **P**-Practical, **T/SDA**-Tutorial / Skill Development Activities (Hours are for Interaction between faculty and students)

1. **Project Work Phase-2:** Students in consultation with the guide/co-guide (if any) in disciplinary project or guides/co-guides (if any) of all departments in case of multidisciplinary projects, shall continue to work of Project Work phase -1to complete the Project work. Each student / batch of students shall prepare project document, and present a seminar.
   CIE marks shall be awarded by a committee comprising of HoD as Chairman, all Guide/s and co-guide/s (if any) and a senior faculty of the concerned departments. The CIE marks awarded for project work phase -2, shall be based on the evaluation of Project Report, Project Presentation skill, and performance in the Question and Answer session in the ratio of 50:25:25.
   SEE shall be at the end of IV semester. Project work evaluation and Viva-Voce examination (SEE), after satisfying the plagiarism check, shall be as per the Institute norms.

Subject	Weeks
Nanotechnology, Science and Applications	8 Weeks
VLSI Interconnects	8 Weeks
Multi-Core Computer Architecture - Storage and Interconnects	8 Weeks
Robotics	8 Weeks
Introduction To Machine Learning - KGP	8 Weeks
Introduction to Industry 4.0 and Industrial Internet of Things	8 Weeks
Introduction to Machine Learning	8 Weeks
Programming, Data Structures and Algorithms Using Python	

VLSI Design

Contact Hours/ Week	:3+2+0(L+P+T)	Credits :	4.0
Total Lecture Hours	: 40	CIE Marks :	50
Total Lab Hours	: 26	SEE Marks :	50
Course Code	: N1LVS01		

Course Objective: This course enables the students to analyze and design combinational, sequential, memory and BiCMOS circuits.

UNIT- I

Introduction: MOS Structure, MOS system under External Bias, Structure and operation of the MOSFET, MOSFET Current-Voltage Characteristics, MOSFET Capacitance.

MOS Inverters- Static Characteristics: Introduction, Resistive-Load Inverter. **08 Hrs**

UNIT- II

Combinational Logic Circuits: Static CMOS inverter, Static behaviour, Propagation delay, Power dissipation, Pseudo NMOS inverter, Static CMOS design, Pass gates, CMOS Transmission Gates, Dynamic CMOS design.

08 Hrs

UNIT- III

Sequential Logic Circuits: Timing metrics for sequential circuits, Static latches and Registers: The Bi-stability principle, Multiplexer based Latches, Master slave edge triggered registers, Static SR Flip-Flops. Dynamic Latches and Registers: Dynamic Transmission gate Edge triggered registers, C^2MOS, True Single Phase Clock Registers (TSPCR).

08 Hrs

UNIT- IV

Arithmetic Building blocks: Adders, Multipliers, Barrel shifter.

Semiconductor Memories: Memory Classification, Non-Volatile Memory devices. Read-Only Memory (ROM) Circuits, **08 Hrs**

UNIT- V

Semiconductor Memories contd.. : Static Read-Write Memory (SRAM) Circuits, Dynamic Read-Write Memory (DRAM) Circuits

BiCMOS Logic Circuits: Introduction, Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.

Chip Input and Output (I/O) Circuits: Introduction, ESD Protection, Input Circuits, Output Circuits and L (di/dt) Noise, On-Chip Clock Generation and Distribution. **08 Hrs**

Text Books:

1	Jan M Rabaey, Anantha Chandrakasan, Borivoje Nikolic	Digital Integrated Circuit A Design Perspective, 2nd Edition, PHI, 2016.
2	Sung Mo Kang & YosufLeblebici,	CMOS Digital Integrated Circuits: Analysis and Design, 4th Edition, Tata McGraw-Hill, 2019.

Reference Books:

1	Neil Weste and K. Eshragian,	Principles of CMOS VLSI Design: A System Perspective, 2nd Edition, Pearson Education (Asia) Pvt. Ltd. 2000.
2	Adel Sedra and Kenneth C. Smith	Microelectronic Circuits Theory and Applications 7th Edition, Oxford Higher Education, 2017.

Course Outcomes: students will be able to

CO1: Analyze the MOS structure and inverter characteristics

CO2: Analyze and design combinational circuits with different design styles.

CO3: Analyze and design sequential circuits with different design systes.

CO4: Analyze and design arithmetic building blocks and Non-Volatile Memory cells.

CO5: Analyze and design Volatile Memory circuits, BiCMOS circuits & Chip I/O circuits.

CO6: Design selected circuit for a perticular application using Mentor graphics. Prepare the report.

<u>Practicals for CIE</u>

- **Design and simulate the following circuits using NG-Spice for the given specifications.**

1. Characterization of NMOS transistor.
2. Design the following static CMOS gates
    a. Inverter
    b. 2-input NAND
    c. 2-input NOR
    d. 2-input XOR
    e. 2-input XNOR.

- **Design (Schematic and Layout) and simulate the following circuits using Mentor graphics or Cadence for the given specifications.**

3. Design the following gates using Static CMOS design style, Pass transistor style and Dynamic gates style.
    a. Inverter
    b. 2-input NAND
    c. 2-input NOR
    d. 2-input XOR
    e. 2-input XNOR.
4. Design a Static CMOS D-register.
5. Design a Static CMOS Full Adder.
6. Design 32 bit adder using the specified topology.
7. Design SRAM.

Analog IC Design

Contact Hours/ Week	:3+0+2(L+P+T)	Credits :	4.0
Total Lecture Hours	: 40	CIE Marks :	50
Total Tutorial Hours	: 26	SEE Marks :	50
Course Code	: N1LVS02		

Course Objective: To impart the knowledge of Analog CMOS IC design for different amplifier topologies.

UNIT – I

Introduction: Introduction to Analog IC design, General concepts - Levels of abstraction, Robustness in Analog design, MOS structure, MOS under external bias, MOSFET: Structure, Threshold voltage, I/V Characteristics, Capacitance. Small signal model.

(08+05) Hrs

UNIT – II

Single stage amplifiers: Common source stage – with resistive load, Diode connected load, current source load, Triode load, Source degeneration. Source follower, Common gate stage, Cascode stage.

(08+05) Hrs

UNIT – III

Differential amplifiers: Single ended differential operation, Basic differential pair, common mode response, Differential pair with MOS loads, Current mirrors: Basic current mirrors, Cascode current mirrors, Active current mirrors.

(08+05) Hrs

UNIT – IV

Frequency response of amplifiers: Miller effect, Association of poles with nodes, CS-stage, Source followers, CG-stage. Feedback: General feedback considerations, Feedback topologies. Two port network models.

(08+06) Hrs

UNIT – V

Operational Amplifier: General considerations, one-stage OP Amps, Two-Stage opamps, Common mode feedback, input range limitations, slew rate, power supply rejection. Stability and Frequency Compensation: General considerations, Multipole systems, Phase margin, Frequency compensation, compensation of two stage op-amps.

(08+05) Hrs

Text Book:

1	Behzad Razavi	Design of Analog CMOS Integrated Circuits 2nd Edition, McGraw Hill Education Private Limited, 2017.

Reference Books:

1	Adel Sedra and Kenneth C. Smith	Microelectronic Circuits Theory and Applications 7th Edition, Oxford Higher Education, 2017.
2	P.R. Gray; P.J. Hurst; S.H. Lewis; R.G. Meyer	Analysis and Design of Analog Integrated circuits, 5th Edition, Wiley, 2009.

Course Outcomes: students will be able to

CO1: Analyze the MOS structure and explain the operation of MOSFET.

CO2: Analyze and design single stage CMOS amplifiers with different loads.

CO3: Analyze and design differential amplifiers and current mirrors with different loads.

CO4: Analyze frequency response of amplifiers and explain the operation of feedback networks.

CO5: Analyze and design operational amplifiers.

ARM Microcontroller and its Applications

Contact Hours/ Week	: 2+0+2 (L+P+T)	Credits :	3.0
Total Lecture Hours	: 26	CIE Marks :	50
Total Tutorial Hours	: 26	SEE Marks :	50
Course Code	: N1LVS03		

Course Objective: To impart the knowledge of Cortex M3 and M4 based Microcontroller Architecture, Exception and Interrupt behavior, Programming and configuring on chip peripherals and interfacing of I/O devices.

UNIT- I

Introduction: Microprocessors and Microcontrollers, Von-Neumann and Harvard Architectures, History of ARM family of processors, Architecture and Features of ARM Cortex M3 and M4 processors. Programmer's model: Operation Modes and States, General purpose Registers, Special function Registers, Behavior of APSR. Pipelining, Prefetch unit and Branch target forwarding in ARM cortex M3 and M4 processors. Memory system: Memory map.

(05+05) Hrs

UNIT- II

Memory Format: Memory endianness, data alignment and unaligned data access support, Bit-band operation in ARM Cortex M3 and M4 processors. Embedded Software development-1: Embedded Software Development and compilation flow. Data types in C – programming used for Cortex M4 processors. Introduction to Cortex M3 based Microcontroller: Features, Memory map, basic configuration and programming of GPIO. Interfacing Input output devices to Cortex M3 based Microcontroller-1: LEDs and Switches, C-Programming examples.

(05+05) Hrs

UNIT- III

Instruction set: Operation and addressing modes of MOV instruction, Arithmetic instructions, Logical instructions, Memory access instructions, Program flow control instructions, Shift and rotate instructions, Data conversion instructions, Bit-field processing instructions, compare and test instructions. Use of suffix in instructions. ARM Assembler directives, Assembly level programming examples. Interfacing Input output devices to Cortex M3 based Microcontroller-2: 7-segment Display, Push button keys, mxn matrix keypad. Programming examples (Both assembly and C).

(05+05) Hrs

UNIT- IV

Embedded Software development-2: Program flow (Software Flow).
Exceptions and Interrupts: Overview of Exceptions and Interrupts, Exception types, Vector table and Reset status, Exception entrance sequence, Exception handler execution, Exception return, Interrupt latency, NVIC registers for interrupt control, Exception handlers in C and assembly level programming, Stack Frames, Exceptions entrance and stacking, Exception return and unstacking. Programming Examples (Both assembly and C). System control blocks of Cortex M3 and M4 based Microcontroller: Reset, Brown-out detection and External interrupt inputs.
Peripherals in Cortex M3 and M4 based Microcontroller: Configuration and programming (both assembly and C) Nested Vectored Interrupt Controller (NVIC) and Timers.

(05+05) Hrs

UNIT-V

Configuration and programming (Only C) PWM unit, Watchdog timer, Analog to Digital Converter (ADC), Digital to Analog Converter (DAC), Universal Asynchronous Receiver Transmitter (UART) , SPI and I2C. Interfacing Input output devices to Cortex M3 and M4 based Microcontroller-3: Stepper Motor, DC motor, Opto-coupler, Relay unit, Programming examples (both assembly and C).

(06+06) Hrs

Text Books:

1	Joseph Yiu	The Definitive guide to ARM Cortex M3 and Cortex M4 processor, Elsevier, 3rd Edition, 2013.
2	Cortex-M Technical Reference Manual. revision r1p1	
3	LPC17xx Reference Manual.	

Reference Book:

1	Ming-Bo Lin	An Introduction to Cortex-M3-Based Embedded Systems: Cortex-M3 Assembly Language Programming, Createspace Independent Publishing Platform, 2019.

Course Outcomes: Students will be able to

CO1: Explain the architecture of ARM cortex M3 and M4 Architecture and differentiate Microcontrollers and Microprocessors.

CO2: Explain the Memory system of ARM Cortex M3 and M4 based Processors and Develop the program for ARM cortex M3 and M4 based microcontrollers in order to Interface Input and output devices such as LED and Switches.

CO3: Explain the operation of the Instruction set of the ARM cortex M3 and M4 based processors and Develop the program for ARM cortex M3 and M4 based microcontrollers in order to Interface Input and output devices such as 7-segment Display, Push button keys, mxn matrix keypad.

CO4: Explain the concept of Exceptions and interrupts and Develop the program to configure peripherals of ARM cortex M3 and M4 based microcontrollers such as External interrupts, NVIC and Timers,

CO5: Develop the program to configure peripherals of ARM cortex M3 and M4 based microcontroller and to develop the program for ARM cortex M3 and M4 based microcontrollers in order to Interface Input and output devices.

Digital System Design Using Verilog

Contact Hours/ Week	: 2+0+2 (L+P+SDA)	Credits :	3.0
Total Lecture Hours	: 26	CIE Marks :	50
Total SDA Hours	: 26		
Course Code	: N1LVS04	SEE Marks :	50

Course Objective: To study and design various digital circuits and systems using Verilog Hardware Description Language (HDL), synthesize and implement on Field Programmable Gate Arrays (FPGAs).

UNIT- I

Introduction to HDL based Digital Design: Design flow and Design styles for digital circuits, Verilog operators, Verilog Primitives, Gate level, Data flow and Behavioural modeling. Delay models, Control statements, Tasks and Functions.

(05+05) Hrs

UNIT- II

Programmable Logic Devices: ROM, PAL, PLA, CPLD, FPGA, FPGA Architecture, FPGA- CLBs, switch Matrix and IOB, Configurable Logic Blocks (CLBs) in Xilinx FPGA –XC3000 and Xilinx Spartan-3, FPGA Design Flow.

FPGA architectures and its usage in embedded Systems: Zynq Ultrascale + MPSoC device architecture. Introduction to Ultrascale Architectecture, System block diagram, High speed serial IO, MIO and EMIO, Functional units and peripherals, Signals interfaces and pins, On chip memory, DMA controller, Reset system, PL peripherals, Vivado design flow, Logic design on Ultrascale + MPSoC FPGA on PL block. Programming and debugging using SDK.

(05+05) Hrs

UNIT- III

Fixed and Floating point Arithmetic: Fixed point number system and floating point number system, Arithmetic operation on Fixed and Floating point numbers.

Combinational circuit design using Verilog:
Ripple Carry adder, Comparators, Combinational Multiplier – Array Multiplier, Unsigned and Signed integer multiplication, Barrel shifter, Tri-State Combinational Circuits.

(05+05) Hrs

UNIT- IV

Sequential Circuit Design using Verilog: Latches, Flip Flops, Shift registers, Counters/ Timers/ Clock Dividers using T Flip Flops, Clock Dividers using D Flip Flops, Synchronous sequential Circuit Design using D and JK Flip Flops.

Finite State Machines (FSM): Finite State Machines and controllers, State diagram, designing FSM using state graph, one-hot-state assignment, controller design. Traffic Light control system.

(05+05) Hrs

UNIT- V

Designing Data path components and Memory units: Serial adder, multiplier using Shift and Add, Fixed point and, Binary Divider, Accumulator, Booth Multiplier, Multiply and Accumulate (MAC) unit, Floating point Multiplier. Memory Design – FIFO, Stack, Circualr Buffer.

(06+06) Hrs

Reference Books:

1	Frank Vahid	Digital Design with RTL Design, VHDL, and Verilog 2nd, Edition John Wiley and SonsPublishers, 2011.
2	Samir Palnitkar	Verilog HDL A guide to Digital Design and Synthesis 2nd Edition, Pearson Education, 2017.
3		Zynq UltraScale+ Device Technical Reference Manual.

Course Outcomes: The students will be able to

CO1: Select appropriate coding style to write Verilog HDL and implement basic combinational circuits to design digital system component.

CO2: Explain the architecture of different FPGAs.

CO3: Design combinational circuits using Verilog HDL and implement on Spartan-3 FPGA.

CO4: Design sequential circuits and State Machine using Verilog HDL and implement on Spartan-3 FPGA.

CO5: Design data path components using Verilog HDL

CO6: Design selected circuit for a particular application using Spartan-3 FPGA. Prepare the report.

Embedded Systems Lab

Lab work Hours/Week	: 1+2+0 (L+P+T)	Credits	:	2.0
Total Lecture Hours Total Lab Hours	: 13 : 26	CIE Marks	:	50
Course Code	: N1LVSL1	SEE Marks	:	50

Course Objectives: This course will enable students to develop assembly level and C-program for Cortex M3 based microcontrollers in order to interface input output devices by configuring on chip peripherals.

List of Experiments –evaluation board:

1. Develop a system to implement a calculator which can perform the operations such as addition, subtraction, Logical AND and Logical OR using 4x4 matrix Keypad/Switches and 16x2 LCD/LEDs interfaced to Cortex M3 based microcontroller. (matrix Keypad, LCD/LED)
2. Develop a system to implement a Traffic control system using on-chip timer and LEDs/7-segment Displays interfaced to Cortex M3 based microcontroller. (Timer, LEDs/7-segment Display)
3. Develop a system to implement a Temperature control system using temperature sensor, on-chip ADC and LCD interfaced to Cortex M3 based microcontrollers. (Signal conditioning circuit, ADC, / LCD, Relay)
4. Develop a system to measure/control the rotation speed of DC motor using on-chip timer/PWM module of Cortex M3 based microcontroller. (PWM, DC motor, Switches)
5. Develop a system to control the direction of rotation and speed of rotation of Stepper motor interfaced to Cortex M3 based microcontroller. (Stepper motor, Switches/ Push button keys)

6. Develop a system to measure the frequency of the input signal/rotation speed of a DC motor interfaced to Cortex M3 based microcontroller. (DC motor, Opto coupler, Timer, LCD)
7. Develop a system to control the bottle filling system using Cortex M3 based microcontrollers. (Stepper motor, IR sensors/Proximity, Solenoid valve)
8. Develop a system to control the Elevator system using Cortex M3 based microcontrollers. (Stepper Motor, Proximity sensor, 7segement Display, Push button keys).
9. Develop a weighing machine using Cortex M3 based microcontrollers. (Signal Conditioning circuit, Load cell, ADC, LCD).
10. Develop a Real time clock using Cortex M3 based Microcontroller. (LCD, Timer).

Open ended Experiments:

1. Develop a Washing machine control unit using Cortex M3 based microcontrollers. (LED, Multiplexed 7-segment display, Keypad, Solenoid valve, Motor control (ON/OFF + Speed), Control logic).

Course Outcomes: Students will be able to

CO1: Develop and execute embedded C and Assembly level programs to interface input/output devices to Cortex M3 based microcontroller.

CO2: Develop and execute embedded C and Assembly level program – Program to configure On-chip peripherals of Cortex M3 based microcontroller.

CO3: Develop embedded System applications using Cortex M3 based microcontroller.

Professional Elective-1

ASIC Design

Contact Hours/ Week	: 2 +0+2(L+P+SDA)	Credits:	3.0
Total Lecture Hours	: 26	CIE Marks:	50
Total SDA Hours	: 26	SEE Marks:	50
Course Code	: N1LVSE11		

Course Objective: To study and design various ASIC configurations, analyze Programmable ASIC memories and Use CAD tools for ASIC design flow.

UNIT- I

Introduction: Types of ASIC Design, ASIC Design Flow, FPGA design Flow, Programmable logic device, ASIC cell libraries.

(05+05) Hrs

UNIT- II

Data Logic Cells: Data Path Elements, Adders, Multiplier, Arithmetic Operator, I/O cell. **ASIC Library Design**: Logical effort: practicing delay, logical area and logical efficiency logical paths, multi stage cells, optimum delay, optimum no. of stages, library cell design.

(05+05) Hrs

UNIT- III

Low-Level Design Entry: Schematic Entry, **Programmable ASIC**: Antifuse, Static RAM, EPROM and EEPROM Technology, FPGA, Programmable ASIC logic cells, ASIC I/O cells, Programmable ASIC Interconnects.

(05+05) Hrs

UNIT- IV

A Brief Introduction to Low Level Design Language: an introduction to EDIF, PLA Tools, an introduction to CFI designs representation. Half gate ASIC. Introduction to Synthesis and Simulation.

ASIC Construction: Physical Design, CAD Tools, System Partitioning, Estimate ASIC size, FPGA Partitioning and its Methods.

(05+05) Hrs

UNIT- V

Floor Planning and Placement and Routing: Physical Design, CAD Tools, System Partitioning, Estimating ASIC size, partitioning methods. Floor planning tools, I/O and power planning, clock planning, placement algorithms. Global Routing, Local Routing, Detail Routing, Special Routing, Circuit Extraction and DRC.

(06+06) Hrs

Text Books:

1	M.J.S .Smith	"Application - Specific Integrated Circuits" – Pearson Education, 2003.
2	Jose E.France, YannisTsividis	"Design of Analog-Digital VLSI Circuits for Telecommunication and signal processing", 2nd Edition, Prentice Hall, 1993.

3	MalcolmR.Haskard; Lan. C. May	“Analog VLSI Design – NMOS and CMOS”, Prentice Hall, 1998.
4	Mohammed Ismail and Terri Fiez	“Analog VLSI Signal and Information Processing”, McGraw Hill, 1994.

Course Outcomes: Students will be able to

CO1: Identify and apply appropriate ASIC configuration for particular application.

CO2: Select and apply appropriate techniques to optimize data path and arithmetic components.

CO3: Identify and use Programmable ASIC memories according to design requirements.

CO4: Use EDIF, PLA tools for synthesis and simulation.

CO5: Use modern CAD tools to design ASICs.

CO6: Design the circuit for a particular application using appropriate tool. Prepare the report.

VLSI Design Automation

Contact Hours/ Week	: 2+0+2 (L+P+SDA)	Credits :	3.0
Total Lecture Hours	: 26	CIE Marks :	50
Total SDA Hours	: 26	SEE Marks :	50
Course Code	: N1LVSE12		

Course Objective: To impart knowledge on implementation of automation methods for VLSI physical design and VLSI interconnects.

UNIT- I

Logic Synthesis & Verification: Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

VLSI Automation Algorithms: Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

(05+05) Hrs

UNIT- II

Placement, Floor Planning & Pin Assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

(05+05) Hrs

UNIT- III

Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches.

(05+05) Hrs

UNIT- IV

Detailed Routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

Over The Cell Routing & Via Minimization: two layers over the cell routers, constrained & unconstrained via minimization.

(05+05) Hrs

UNIT- V

Scripting Languages: Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables. Inter process Communication Threads, Compilation & Line Interfacing.

(06+06) Hrs

Text Books:

1	NaveedShervani	Algorithms for VLSI physical design Automation, Kluwer Academic Publisher, 3rd Edition, 1998
2	ChristophnMeinel & Thorsten Theobold	Algorithm and Data Structures for VLSI Design, KAP, 2002.
3	Rolf Drechsheler	Evolutionary Algorithm for VLSI, Springer, 2nd Edition, 2013.
4	Trimburger	Introduction to CAD for VLSI, Kluwer Academic publisher, 1st Edition, 2002.
5	Randal L, Schwartz Tom Phoenix	Learning PERL, Oreilly Publications, 3rd Edition, 2000.
6	Larry Wall, Tom Christiansen, John Orwant	Programming PERL, Oreilly Publications, 3rd. Edition, 2000.
7	Tom Christiansen, Nathan Torkington	"PERL Cookbook, Oreilly Publications, 3rd Edition, 2000.

Course Outcomes: Students will be able to,

CO1: Identify and discuss partitioning algorithms used to design VLSI automation and explain the basic concepts of Logical high level synthesis and verification of hardware models

CO2: Discuss the placement and floor planning algorithms.

CO3: Select suitable routing algorithms in VLSI design automation.

CO4: Classify routing algorithms with respect to different layers.

CO5: Discuss script languages for VLSI design automation.

CO6: Design the circuit for a particular application using appropriate tool. Prepare the report.

VLSI for Digital Signal Processing

Contact Hours/ Week	: 2 +0+2(L+P+T)	Credits :	3.0
Total Lecture Hours	: 26	CIE Marks :	50
Total Tutorial Hours	: 26	SEE Marks :	50
Course Code	: N1LVSE13		

Course Objective: To study the methodologies needed to design custom or semi-custom VLSI circuits for Signal Processing applications

UNIT- I

Iteration Bounds:

Introduction: DSP algorithms: FIR and IIR Filters, Representation of DSP Algorithms.

Iteration Bounds: loop bound and Iteration bound, Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs.

(05+05) Hrs

UNIT- II

Pipelining and parallel processing: pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power.

Retiming: Definition and Properties, Solving Systems of Inequalities, Retiming Techniques.

(05+05) Hrs

UNIT- III

Unfolding: An Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Applications of Unfolding.

(05+05) Hrs

UNIT- IV

Systolic architecture design: systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design.

(05+05) Hrs

UNIT- V

Fast convolution–Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution,

Pipelined and Parallel recursive filter: Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing

(06+06) Hrs

Text Book		
1	KeshabK.Parthi	"VLSI Digital Signal Processing systems, Design and implementation ", Wiley, Inter Science, 1999.
Reference Books:		
1	Mohammed Isamail and Terri Fiez	Analog VLSI Signal and Information Processing, Mc Graw-Hill, 1994.
2	S.Y. Kung, H.J. White House, T. Kailath	VLSI and Modern Signal Processing, Prentice Hall, 1985.
3	Jose E. France, YannisTsividis	Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing, Prentice Hall, 1994.

Course Outcomes: The students will be able to

CO1: Explain various DSP algorithms and represent algorithms using block diagrams, signal flow graphs and data flow graphs.

CO2: A. Compute the iteration bound using Longest Path Matrix Algorithm and the Minimum Cycle Mean Algorithm.

B. Calculate critical path computation time and power consumption in filters

CO3: Perform retiming in filters and decide different retiming techniques and algorithm for unfolding.

CO4: Explain Systolic architecture design methodologies

CO5: Apply various algorithms for efficient implementation of convolution Apply pipelining and parallel processing for implementing filters.

ACADEMIC YEAR: 2022-23

Nano Electronics

Contact Hours/ Week	: 2+0+2(L+P+SDA)	Credits :	3.0
Total Lecture Hours	: 26	CIE Marks :	50
Total SDA Hours	: 26	SEE Marks :	50
Course Code	: N1LVSE14		

Course Objective: This course will enable students to understand various advanced concepts in nanoelectronics and the fundamentals on QED, SED, Molecular electronics and spintronics along with computational tools for modelling and simulation of nanoelectronics devices.

UNIT – I

Introduction to Nanoelectronics: Limitations of the conventional MOSFETs at Nanoscales, MOSFET Scaling & implications, Introductory concepts of Ballistic transport and Quantum confinement, Differences in Few Electron Devices (as analog version) and Single Electron Devices (as digital version) of Nanoelectronic devices

Nanostructures and Quantum Electronic Devices: Low-dimensional structures- Quantum wells, Quantum wires and Quantum dots; Density of states in low-dimensional structures; Quantum Interference Devices; Split – Gate Transistor; Electron – Wave Transistor; Resonant tunneling phenomena and its applications in diodes and transistors

(05+05) Hrs

UNIT – II

Molecular Electronic: Overview & Basics; Fabrication of molecular electronics-based transistor devices; Conductivity of organic polymers-Conduction mechanism in organic polymers; Polymer Electronics; Self-Assembling Circuit.

(05+05) Hrs

UNIT – III

Single Electron Devices: Principle of operation- Single-Electron Effect, Coulomb Blockade Phenomenon; Theoretical Quantum Dot Transistor - Energy of Quantum Dot system, Single-Electron Quantum-Dot Transistor, Single transistors; Conductance Oscillation and Potential Fluctuation; Transport under Finite temperature and Finite Bias; Coulomb Blockade Devices.

(05+05)Hrs

UNIT – IV

Carbon Nanoelectronics: Carbon nanotubes - SWCNTs and MWCNTs; 1D quantization in nanotubes- van Hove singularities; Fabrication of CNTs; CNT FETs- Device characteristics, CNT-TUBFET, CNT-SET; and NanoWire FETs; Electronic structure of graphene; Graphene FETs- GNRFETs.

(05+05) Hrs

UNIT – V

Spintronics: Fundamentals of spintronics; Spintronic devices- spin diodes and spin transistors

Current Nanoelectronic Devices: Quantum Effects in MOSFETs, Strained Silicon, Fully Depleted SOI-MOSFET, Double-Gate MOSFET, Multi-gate MOSFETs, FIN-FET, Electrically Induced Junctions for EJ-MOSFETs, Ballistic Transport, Conductance Quantization, Quantum Point Contact Devices. **(06+06) Hrs**

Text Books:

1	Shunri Oda, David Ferry	Nanoscale Silicon Devices, CRC Press, Taylor & Francis Group, 2015.
2	K. Goser, P. Glosekotter	Nanoelectronics and Nanosystems, Springer, 2005

Reference Books:

1	Suprio Datta	Lessons from nanoelectronics, World Scientific publisher, 2015
2	Karl Goser, Peter Glosekotter, Jan Dienstuhl	Nanoelectronics and Nanosystems- From Transistors to Molecular and Quantum Devices, Springer-Verlag 2004.
3	C.N.R. Rao and A. Govindaraj	Nanotubes and nanowires, RSC Publishing, 2005.
4	Konstantin K. Likharev	Single Electron Devices and their Applications, IEEE proceedings, vol. 87, no. 4, April 1999.p 606- 632
5	Ziese and M. J. Thornton	Spin Electronics, Springer-Verlag, 2001.
6	Supriyo Datta	Quantum Transport-From Atom to Transistor, Cambridge University press, 2005.

Course Outcomes: Students will be able to

CO1: Gain the concepts of nanoelectronics such as ballistic transport and quantum confinement.

CO2: Understand various nanostructures and its applications towards Quantum Electronic Devices.

CO3: Acquire the fundamentals of Molecular Electronics

CO4: Obtain the knowledge of Single Electron Devices and carbon based nanoelectronic devices.

CO5: Learn the fundamentals of Spintronics.

CO6: Design and simulate various advanced nanoelectronic devices.

II Semester

SIDDAGANGA INSTITUTE OF TECHNOLOGY, TUMAKURU-03

(An autonomous Institute under Visvesvaraya Technological University)

SCHEME OF TEACHING AND EXAMINATION

II SEMESTER M.Tech. VLSI Design and Embedded Systems

Sl. No.	Course Type and Course Code		Course Title	Teaching Hours per Week			Examination				Credits
				Theory	Practical / Seminar	Tutorial / Skill Development Activities	Duration in hrs.	CIE Marks	SEE Marks	Total Marks	
				L	P	T/SDA					
1.	IPCC	N2LVS01	Real time operating systems	3	2	0	3	50	50	100	4
2.	PCC	N2LVS02	VLSI Process Technology	3	0	2	3	50	50	100	4
3.	PCC	N2LVS03	Design of IoT Systems	2	0	2	3	50	50	100	3
4.	PEC	N2LVSE2x	Professional Elective – 2	2	0	2	3	50	50	100	3
5.	PEC	N2LVSE3x	Professional Elective – 3	2	0	2	3	50	50	100	3
6.	OEC	N2OExx	Open Elective	3	0	0	3	50	50	100	3
7.	MPS	N2LVSMPS	Mini Project with Seminar	0	4	2	--	100	--	100	3
8.	PCCL	N2LVSL1	VLSI DESIGN LAB	1	2	0	3	50	50	100	2
9.	AEC	ARAS	Aptitude Related Analytical Skills	36 Hrs. for the entire semester			2	50	50	100	0
10	AUD/ AEC	N2LVSAUD / N2LVSAEC	BoS Recommended online course	Classes and Evaluation Procedures are as per the policy of the online course providers							0
	Total			**16**	**8**	**10**		**500**	**400**	**900**	**25**

Note: **IPCC**-Integrated Professional Core Courses, **PCC**: Professional Core Course, **PEC:** Professional Elective Course, **OEC**- Open Elective Course, **MPS**- Mini Project with Seminar, **PCCL**-Professional Core Course Lab, **AUD/AEC** –Audit Course / Ability Enhancement Course (A pass in AUD/AEC is mandatory for the award of the degree) **L**-Lecture, **P**-Practical, **T/SDA**-Tutorial / Skill Development Activities (Hours are for Interaction between faculty and students)

Professional Elective 2		**Professional Elective 3**		**Open Elective 1**	
N2LVSE21	CMOS RF Circuit Design	N2LVSE31	System on Chip (SoC) Design	N2OE01	Embedded Systems
N2LVSE22	Mixed Signal Circuit Design	N2LVSE32	System Verilog	N2OE02	CMOS RF Circuit Design
N2LVSE123	VLSI Testing and Verification	N2LVSE33	Low power VLSI Design		
N2LVSE24	Design of CMOS Phase Locked Loops.	N2LVSE34	Wireless sensor network		
N2LVSE25	DSP Architecture	N2LVSE35	Interface and Noise control technique in Electronic System design		

1. **Mini Project with Seminar:** This may be hands-on practice, survey report, data collection and analysis, coding, mobile app development, field visit and report preparation, modelling of system, simulation, analysing and authenticating, case studies, etc.
   CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide, if any, and a senior faculty of the department. Students can present the seminar based on the completed mini-project. Participation in the seminar by all postgraduate students of the program shall be mandatory.
   The CIE marks awarded for Mini-Project work and Seminar, shall be based on the evaluation of Mini Project work and Report, Presentation skill and performance in Question and Answer session in the ratio 50:25:25. Mini-Project with Seminar shall be considered as a head of passing and shall be considered for vertical progression as well as for the award of degree. Those, who do not take-up/complete the Mini Project and Seminar shall be declared as fail in that course and have to complete the same during the subsequent semester. **There is no SEE for this course.**
2. **Internship:** All the students shall have to undergo a mandatory internship of **06 weeks** during the vacation of II and III semesters. A University examination shall be conducted during III semester and the prescribed internship credit shall be counted in the same semester. The internship shall be considered as a head of passing and shall be considered for vertical progression as well as for the award of degree. Those, who do not take-up/complete the internship shall be declared as fail in the internship course and have to complete the same during the subsequent University examination after satisfying the internship requirements.

Real Time Operating Systems

Contact Hours/Week	: 3+2+0 (L+P+T)	Credits :	4.0
Total Lecture Hours	: 40	CIE Marks :	50
Total Lab Hours	: 26	SEE Marks :	50
Course Code	: N2LVS01		

Course Objectives: To introduce the students with basics of real-time systems , knowledge and skills necessary to design and develop embedded applications by using real-time operating systems.

UNIT- I

Introduction to Real-Time Embedded Systems: Brief history of Real Time Systems, A brief history of Embedded Systems.

System Resources: Resource Analysis, Real-Time Service Utility, Scheduling Classes, The Cyclic Executive, Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies, Real-Time OS, Thread Safe Reentrant Functions.

Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility.

08 Hrs

UNIT- II

Processing: Deadline – Monotonic Policy, Dynamic priority policies.

I/O Resources: Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture.

Memory: Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash file systems. **08 Hrs**

UNIT- III

Multi-resource Services: Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion.

Soft Real-Time Services: Missed Deadlines, QOS.

Soft Real-Time Services: Alternatives to rate monotonic policy, mixed hard and soft real-time services.

Embedded System Components: Firmware components, RTOS system software mechanisms, Software application components. **08 Hrs**

UNIT- IV

Firmware Components: The 3 firmware components, RTOS system software mechanisms, Software application components.

Debugging Components: Exceptions, assert, Checking return codes. Single-step debugging, kernel scheduler traces, Test access ports, Trace ports, Power-On self test and diagnostics, External test equipment, Application-level debugging.

Performance Tuning: Basic concepts of drill-down tuning, hardware – supported profiling and tracing, Building performance monitoring into software, Path length, Efficiency Call frequency, Fundamental optimizations. **08 Hrs**

UNIT- V

High availability and Reliability Design: Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design tradeoffs, Hierarchical applications for Fail-safe design.

Process and Threads: Process and thread creations, Programs related to semaphores, message queue, shared buffer applications involving inter task/thread communication **08 Hrs**

Reference Books:

1	Sam Siewert	"Real-Time Embedded Systems and Components" Cengage Learning India Edition, 2007.
2	Myke Predko	"Programming and Customizing the PIC microcontroller" 3rd Ed, TMH, 2008.
3	Dreamtech Software Team,Jhon Wiley, India Pvt. Ltd.	"Programming for Embedded Systems" 2008.

Course Outcomes: The student will be able to

CO1: Understand the fundamental concepts of real-time operating systems

CO2: Analyze the system resources required to build RTOS.

CO3: Analyze the Multi-service resources required for RTOS

CO4: Analyze various performance tuning techniques

CO5: Analyze avilability and reliability design issuses, Develop programs for multithreaded applications using suitable techniques.

CO6: Write C programs to create multithreads and demonstrate the working

Practicals for CIE

1. Creation of multithreads
2. Assigning different priorities to threads
3. Threads with same priority
4. Priority inheritence
5. Communication between Parent and child thread.
6. Shared recourse and Semaphore to manage shared recourse
7. Communication between a pipe server and a process thread
8. PROSIX based message Queue
9. Real time Camera interfacing.

VLSI Process Technology

Contact Hours/ Week	: 3+0+2 (L+P+SDA)	Credits :	4.0
Total Lecture Hours	: 40	CIE Marks :	50
Total SDA Hours	: 26	SEE Marks :	50
Course Code	: N2LVS02		

Course objective: This course aims at understanding the manufacturing methods and their underlying scientific principles in the context of technologies used in VLSI chip fabrication.

UNIT- I

Introduction: Electronic-Grade Silicon, Czochralski Crystal Growing, Silicon Shaping, Process Considerations. Environment for VLSI technology: clean room and safety requirements, Wafer cleaning process.

Epitaxy: Introduction, Vapour-Phase Epitaxy, Molecular Beam Epitaxy, Epitaxial Evaluation.

Oxidation: kinetics of silicon dioxide growth for thick, thin and ultra-thin films. Oxidation technologies in VLSI and ULSI; Characterization of oxide films; high K and low K dielectrics for VLSI. **08 Hrs**

UNIT- II

Chemical Vapour deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride.

Metallization: Metallization Applications, Metallization Choices, Physical Vapor Deposition (evaporation and sputtering techniques). Failure mechanisms in metal interconnect; multilevel Metallization schemes, New Role of Metallization. **08 Hrs**

UNIT- III

Impurity incorporation: Models of **Diffusion** in Solids, Fick's laws for Diffusion, Measurement Techniques, Fast Diffusion in Silicon.

Ion implantation: Introduction, Range Theory, Implantation Equipment, Annealing, Shallow Junctions, High-Energy Implantation, annealing; Characterization of impurity profiles.

Reactive Plasma Etching: Introduction, Plasma Properties, Feature-Size Control and Anisotropic Etch Mechanisms, Other Properties of Etch Processes, Reactive Plasma-Etching Techniques and Equipment, Specific Etch Processes. **08 Hrs**

UNIT- IV

Lithography: Introduction, Optical Lithography, Electron Lithography, X-ray Lithography, Ion Lithography.

Thin film Characterization: Overview of thin film characterization, **Imaging** techniques: Scanning electron microscopy (SEM), AFM, **Structural** properties: X-ray diffraction (XRD), **Electrical** properties: Resistance/resistivity – four point probe, Vander Pauw, **Mechanical** properties: Stress-curvature measurements**.** **08 Hrs**

UNIT- V

VLSI Process Integration: Introduction, Fundamental Considerations for IC Processing, NMOS IC technology, CMOS IC Technology, MOS Memory IC Technology, Bipolar IC Technology, IC Fabrication.

Packaging of VLSI Devices: Introduction, Package Types, Packaging Design Considerations. **08 Hrs**

Text Books:

1	S. M. Sze,	VLSI Technology, McGraw-Hill, 2nd Edition, 1998.
2	S.K. Ghandhi,	VLSI Fabrication Principles, John Wiley Inc., New York, 2nd Edition, 2008.
3	John A. Venables	Introduction to Surface and Thin Films Processes, Cambridge University Press, 2000.
4	Leon I. Maissel and Reinhard Glang.	Handbook of Thin Film Technology, McGraw-Hill Publishing Company, New Delhi (1970)

Course Outcomes: students will be able to

CO1: Identify and describe the various processes present in the crystal growth and wafer preparation for Electron grade Silicon. Select appropriate epitaxial growth techniques employed in IC's fabrications and discuss each process.

CO2: Select and discuss an appropriate chemical vapor deposition method to deposit polySi, SiO_2 and SiN_3 thin films and metallization process for IC's fabrications.

CO3: Identify and select appropriate impurity incorporation, annealing techniques and reactive plasma etching methods used in IC's fabrications

CO4: Identify, select and discuss the various lithography techniques used in IC's fabrications. Identify, select and discuss the various characterization techniques (the structural, electrical and mechanical properties) used analyzing the material properties of thin films.

CO5: Identify and explain the various IC fabrication process sequence and special considerations. Select an appropriate package type and explain design considerations of VLSI devices.

CO6: Deposit the material in thin film using PVD technique and analyze the properties of the deposited film using various characterization techniques in a team. Prepare the report.

List of Activities for CIE.

1. Silicon wafer Cleaning (RCA1 and RCA2)
2. Glass Substrate cleaning
3. Deposition of insulating material (Al2O3/ SiO2) on Si/glass substrate using E – beam Evaporation.
4. Deposition of metal/ alloys on insulated Si/glass substrate using DC Sputtering.
5. Deposition of semiconductor on insulated Si/glass substrate RF Sputtering
6. Analyse the structural properties of deposited thin film using XRD and AFM/SEM.
7. Determination of sheet resistance of deposited thin film using 4 probe method.

Design of IoT Systems

Contact Hours/ Week	: 2 +0+2 (L+P+SDA)	Credits:	3.0
Total Lecture Hours	: 26	CIE Marks:	50
Total SDA Hours	: 26	SEE Marks:	50
Course Code	: N2LVS03		

Course Objective: To impart the knowledge of components, Communication and development of software required for the design of IoT systems.

UNIT- I

Definition and Characteristics of IoT, IoT architectures and Reference Models, A core IoT functional Stack, Data management and Compute stack. Introduction to the IoT Framework: A brief refresher on the Internet, Communication models and Communication APIs, The IoT Framework, Types of IoT Systems, Challenges of implementing Effective IoT Systems. IoT Levels and Deployment Templates.

(05+05) Hrs

UNIT- II

Basic Python Programming: Python Data types and Data structures, Control flow, Functions, Modules, Packages, File Handling, Data/Time operations, Classes , Python Packages of Interest for IoT.

(05+05) Hrs

UNIT- III

IoT Physical Devices and End points: Introduction to Renesas Synergy kits, Arduino and Raspberry pi boards. Introduction to Sensors, Actuators and Smart objects/sensors, IoT Design methodology.

(05+05) Hrs

UNIT- IV

Connecting smart objects: Communications criteria, Wireless sensor networks and its Technologies, Bluetooth, Wi-Fi, Zigbee, LoRa, RFID, IoT Access Technologies. IP as the IoT Network layer, Advantages of internet Protocol(IP), Adoption and Adaption of the IP, Optimizing IP for IoT.

(05+05) Hrs

UNIT- V

IoT protocols: MQTT, XMPP, DDS, AMQP, COAP, REST. Cloud services for IoT(AWS). IoT Web application development: HTML, CSS, JavaScript, MongDB, Python web application framework: Django. Case studies: case study on IoT System for Weather monitoring, Home Automation, Agriculture, Industry.

(06+06) Hrs

Text Books:

1	Arshdeep Bahga, Vijay Madisetti	Internet of Things , A Hands on Approach 1st Edition, 2015.
2	David Hanes, Gonzalo Salgueiro,Patrick Grossetete, Robert Barton, Jerome Henry	IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things, Pearson Education (Cisco Press Indian Reprint), (ISBN: 978-9386873743), 1st Edition, 2017.
3	Sammi salama hussen Hajjaj, Kisheen Rao	The Intenet of Mechanical Things: The IoT Framework for Mechanical Engineers., CRC

	Gsangaya	press Taylor and Francis Group, 1st Edition 2022,
4	Srinivasa K Srinivasa K.G., Siddesh G.M., Hanumantha Raju R.	Internet of Things, Cengage learning India 1st Edition, 2018.

Course Outcomes: Students will be able to

CO1: Explain the building blocks of an IoT system.

CO2: Develop Python programmes and use python packages related to IoT.

CO3: Explain the IoT Design methodology and the operation of end point devices such as Renesas Synergy kits, Arduino and Raspberry Pi.

CO4: Explain the concept of Wireless sensor networks and different technologies used for IoT.

CO5: Explain the operation of IoT protocols, develop web applications and prepare case studies for IoT based applications.

CO6: Design the circuit for a particular application using appropriate tool. Prepare the report.

VLSI Design Lab

Lab work Hours/Week	: 1+2+0 (L+P+T)	Credits	:	2.0
Course Code	: N2LVSL1	CIE Marks	:	50
		SEE Marks	:	50

Course Objective: Analyse, Design and simulate digital and analog MOSFET circuits for various applications.

List of Experiments:

1. Design a given logical operation using CMOS design style.
a. Draw the schematic and verify the design parameters with the help of
   i. Transient Analysis to verify the truth table
b. Draw the Layout and verify the DRC.
c. Extract RC and back annotate the same and verify the Design
2. Design a CMOS full adder for given specifications.
a. Draw the schematic and verify the design parameters with the help of
   i. Transient Analysis to verify the truth table
b. Draw the Layout and verify the DRC.
c. Extract RC and back annotate the same and verify the Design

3. Design a Common Source amplifier with resistive load for given specifications.

a. Draw the schematic and verify the design parameters with the help of
   i. DC Analysis (Calculate the theoretical value for Av)
   ii. Transient Analysis (Verify theoretical value of Av with its Practical value).

b. Draw the Layout and verify the DRC, LVS

c. Extract RC and back annotate the same and verify the Design

4. Design a Common Source amplifier with Active load using Current mirror for given specifications.
   Complete the design flow mentioned below:

a. Draw the schematic and verify the design parameters with the help of
   i. DC Analysis (Calculate the theoretical value for Av)
   ii. Transient Analysis (Verify theoretical value of Av with its Practical value).

b. Draw the Layout and verify the DRC, LVS

c. Extract RC and back annotate the same and verify the Design

5. Design a Common drain amplifier with Active load for given specifications.

Complete the design flow mentioned below:

a. Draw the schematic and verify the design parameters with the help of
   i. DC Analysis (Calculate the theoretical value for Av)
   ii. Transient Analysis (Verify theoretical value of Av with its Practical value).

b. Draw the Layout and verify the DRC, LVS

c. Extract RC and back annotate the same and verify the Design

6. Design a Differential Amplifier with Active load using Current mirror for given specifications.

Complete the design flow mentioned below:

a. Draw the schematic and verify the design parameters with the help of
   i. DC Analysis (Calculate the theoretical value for Av)
   ii. Transient Analysis (Verify theoretical value of Av with its Practical value).

b. Draw the Layout and verify the DRC, LVS.

c. Extract RC and back annotate the same and verify the Design.

7. Design a Operational Amplifier with Active load using Current mirror for given specifications.

Complete the design flow mentioned below:

a. Draw the schematic and verify the design parameters with the help of

i. DC Analysis
ii. Transient Analysis

b. Draw the Layout and verify the DRC, LVS
c. Extract RC and back annotate the same and verify the design

8. Design a 4 bit binary weighted DAC / 4-bit R-2R Ladder DAC for given specifications.
   Complete the design flow mentioned below:

a. Draw the schematic and verify the design parameters with the help of
   i. DC Analysis
   ii. Transient Analysis
b. Draw the Layout and verify the DRC, LVS
c. Extract RC and back annotate the same and verify the design

Course Outcomes: Student will be able to

CO1: Analyze and Design analog circuits and also simulate the same using EDA tool and prepare the report.

CO2: Analyze and Design digital circuits and also simulate the same using EDA tool and prepare the report.

Professional Elective- 2

CMOS RF Circuit Design

Contact Hours/ Week	: 2+0+2(L+P+T)	Credits :	3.0
Total Lecture Hours	: 26	CIE Marks :	50
Total Tutorial Hours	: 26	SEE Marks :	50
Course Code	: N2LVSE21		

Course Objective: To impart the knowledge on designing CMOS RF Circuit.

UNIT- I

Introduction to RF Design and Wireless Technology: Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Intersymbol interference, random processes and noise, Sensitivity and dynamic range, conversion of gains and distortion, characteristics of passive IC components, resistor, capacitor and inductor. **(05+05) Hrs**

UNIT- II

RF Modulation: Analog Modulation: Amplitude Modulation, Phase and Frequency Modulation, Digital modulation: Basic concepts, Binary Modulation, Quadrature Modulation. Power efficiency of modulation schemes, Coherent and Non-coherent detectors. Mobile RF communication, basics of multiple access techniques and wireless standards. **(05+05) Hrs**

UNIT- III

Transceiver Architectures: Receiver Architecture: Heterodyne, Homo dyne, Image Reject Receiver and Transmitter Architecture.

Distributed Systems: Transmission lines, reflection coefficient, the wave equation, examples, Lossy transmission lines, Smith charts – plotting gamma.

High Frequency Amplifier Design: Bandwidth estimation using open-circuit time constants, Bandwidth estimation using short-circuit time constants, Rise time, delay and bandwidth, Zeros to enhance band width, Shunt-series amplifiers, tuned amplifiers, and Cascaded amplifiers.

(05+05) Hrs

UNIT- IV

Low noise Amplifier design: CS stage: Inductive load, Resistive Feedback, Inductive degeneration. Variants of CS LNA, Noise – Cancelling LNAs, Differential LNAs. Non linearity Calculations in LNAs.

Mixers: Mixer Nose Figures, Port – Port Feed through, Single –balanced and double balanced Mixers, Introduction to Passive and Active Mixers.

(05+05) Hrs

UNIT- V

Oscillators: General Principles: Feedback view, One-Port view, Cross-Coupled Oscillator, Three – Point Oscillators. Voltage Controller Oscillators (VCO): Tuning Limitations, Effect of varactor Q, VCOs with wide tuning Range. Effect of Phase Noise, Low noise VCOs.

Phase Locked Loop (PLL): Type – I PLLs: VCO phase Alignment, Dynamics of Type – 1 PLLs, Frequency Multiplication, Draw backs of Type – 1 PLL. Type-II PLLs: Phase/Frequency Detectors, Charge Pumps, Charge-Pump PLLs, Transient Response.

Integer N Frequency Synthesizer: Basic integer N Frequency Synthesizer, Setting behavior, Spur reduction technique. **(06+06) Hrs**

Text Books:

1	B. Razavi	RF Microelectronics, PHI, 2nd Edition, 2011
2	R. Jacob Baker, H.W. Li, D.E. Boyce	CMOS Circuit Design, layout and Simulation, PHI, 1998.
3	Thomas H. Lee	Design of CMOS RF Integrated Circuits Cambridge University press, 2nd Edition, 2003.
4	Y.P. Tsividis	Mixed Analog and Digital Devices and Technology, TMH, 1996

Course Outcomes: Students will be able to,

CO1: Explain performance parameters to be considered for the design of RF circuits.

CO2: Identify, select and explain the modulations technique and RF communication concepts for RF circuit design.

CO3: Discuss various Transceiver architecture and bandwidth estimation techniques.

CO4: Identify and explain the general considerations of low noise amplifiers and concepts of mixers.

CO5: Discuss the modeling of various devices at RF Frequency and general principles of oscillators and PLL. Design RF modulation modules and various amplifiers using Matlab Simulink. Prepare the report.

Mixed Signal Circuit Design

Contact Hours/ Week	: 2+2+0 (L+P+T)	Credits :	3.0
Total Lecture Hours	: 26	CIE Marks :	50
Total Tutorial Hours	: 26	SEE Marks :	50
Course Code	: N2LVSE22		

Course objective: This course aims at understanding the various integrated based filters, data converters, integrated circuit of oscillators and PLLs in IC design

UNIT- I

Submicron CMOS Circuit Design

Submicron CMOS: Overview and Models, CMOS process flow, Capacitors and Resistors. Digital circuit design: The MOSFET Switch, Delay Elements, An Adder. Analog Circuit Design: Biasing, Op-Amp Design, Circuit Noise.

(05+05) Hrs

UNIT- II

Integrator Based CMOS Filters

Integrator Building Blocks- low pass filter, Active RC integrators, MOSFET-C Integrators, gm- C integrators, Discrete time integrators. Filtering Topologies: The Bilinear transfer function, The Biquadratic transfer function, Filters using Noise shaping.

(05+05) Hrs

UNIT- III

Data Converter Architectures

DAC Architectures- Resistor string, R-2R ladder Networks, Current Steering, Charge Scaling DACs, Cyclic DAC, and Pipeline DAC. ADC

Architectures- Flash, Two-step flash ADC, Pipeline ADC, Integrating ADC's, Successive Approximation ADC.

(05+05) Hrs

UNIT- IV

Data Converter Modeling and SNR

Sampling and Aliasing: A modeling approach, Impulse sampling, The sample and Hold, Quantization noise. Data converter SNR: An overview, Clock Jitter, Improving SNR using Averaging, Decimating filter for ADCs, Interpolating filter for DACs, Band pass and High pass sinc filters - Using feedback to improve SNR.

(05+05) Hrs

UNIT- V

Oscillators and PLL

LC oscillators, Voltage Controlled Oscillators. Simple PLL, Charge pumps PLLs, Non ideal effects in PLLs, Delay Locked Loops.

(06+06) Hrs

Course Outcomes: students will be able to

CO1: Apply the concepts for mixed signal MOS circuit.

CO2: Analyze the characteristics of IC based CMOS filters.

CO3: Design of various data converter architecture circuits.

CO4: Analyze the signal to noise ratio and modeling of mixed signals.

CO5: Design of oscillators and phase lock loop circuit.

Text Books:

1	R.Jacob Baker	CMOS Mixed Signal Circuit Design, Wiley India, IEEE Press, reprint 2008.
2	R.Jacob Baker	CMOS Circuit Design, Layout and Simulation, Wiley India, IEEE Press, 2nd Edition, reprint 2009.
3	Behzad Razavi	Design of Analog CMOS Integrated Circuits, McGraw Hill, 33rd Re- print, 2016.

VLSI Testing and Verification

Contact Hours/ Week	: 2+0+2 (L+P+SDA)	Credits :	3.0
Total Lecture Hours	: 26	CIE Marks :	50
Total SDA Hours	: 26	SEE Marks :	50
Course Code	: N2LVSE23		

Course Objective: This course introduces methods to fault model and generate tests for digital circuits and discuss various verification tools.

UNIT- I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing.**Faults:** Single Stuck at faults, Temporary Faults. Bridging faults, Transient faults.
Fault modeling: Fault equivalence, dominance and collapsing.
Fault Simulation: parallel, concurrent and deductive simulation.

(05+05) Hrs

UNIT- II

Test Generation for Combinational Logic Circuits: Test Generation Techniques for Combinational Circuits: Truth table method, Fault matrix method, Boolean difference method, Path sensitization method, D-Roth algorithm, PODEM and FAN. Detection of Multiple Faults in Combinational Logic Circuits.

(05+05) Hrs

UNIT- III

Design of Testable Sequential Circuits: Controllability and Observability, Ad Hoc Design Rules for Improving Testability, The Scan-Path Technique for Testable Sequential Circuit Design, Level-Sensitive Scan Design, Random Access Scan Technique, Partial Scan, Testable Sequential Circuit Design Using Nonscan Techniques, Crosscheck, Boundary Scan.

(05+05) Hrs

UNIT- IV

Built-In Self Test: Test Pattern Generation for BIST, Output Response Analysis, BIST Architectures-BILBO.
Testable Memory Design: RAM Fault Models, Test Algorithms for RAMs:March algorithm(Row, Column), galloping algorithm, butterfly algorithm,Neighbourhood Pattern Sensitive Faults(NPSF), Detection of Pattern Sensitive Faults, BIST Techniques for Ram Chips, Test Generation and BIST for Embedded RAMs.

(05+05) Hrs

UNIT- V

Importance of Design Verification: The importance of verification, Reconvergence model, Formal verification, Assertion based verification, Equivalence checking, Model checking, Functional verification.

Verification Tools: Linting tools: Limitations of linting tools, lintingverilog source code, linting VHDL source code, lintingOpenVera and e-source code, code reviews.

Simulators: Stimulus and response, Event based simulation, cycle based simulation, Co-simulators, verification intellectual property: hardware modelers, waveform viewers.

Verification plan: The role of verification plan: specifying the verification plan, Levels of verification: unit level verification, reusable components verification, ASIC and FPGA verification, system level verification, board level verification. **(06+06)Hrs**

Text Books:

1	P. K. Lala	Digital Circuit Testing and Testability, Academic Press, 1997.
2	M.L. Bushnell and V.D. Agrawal	Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Springer, 1st Corrected Edition 2002, Corr. 2nd printing 2004 edition, 2005.
3	M. Abramovici, M.A. Breuer and A.D. Friedman	Digital Systems and Testable Design, Jaico Publishing House, 1st Edition, 2001.
4	JanickBergeron,	Writing testbenches: functional verification of HDL models, Kluwer Academic Publishers, 2nd Edition , 2003
5	JayaramBhasker, RakeshChadha	Static Timing Analysis for Nanometer Designs: A practical approach, Springer publications, 2009.
6	PrakashRashinkar PeterPaterson, LeenaSingh	System on a Chip Verification, Springer, 2002nd edition, 2000.

Course Outcomes: Students will be able to

CO1: Identify and generate test for the faults in digital circuits. Identify and apply the appropriate test generation technique for combinational circuits.

CO2: Identify and apply the appropriate Ad Hoc techniques to improve testability of sequential circuits.

CO3: Select appropriate algorithms to test memory elements.

CO4: Discuss verification plan and verification tools.

CO5: Analyze the circuits for static timing verification. Design software algorithm or hardware circuit to test the ICs.Prepare report on the same.

CO6: Design the circuit for a particular application using appropriate tool. Prepare the report.

Design of CMOS Phase Locked Loops

Contact Hours/ Week	: 2+0+2(L+P+T)	Credits :	3.0
Total Lecture Hours	: 26	CIE Marks :	50
Total Tutorial Hours	: 26	SEE Marks :	50
Course Code	: N2LVSE24		

Course Objective: To impart the knowledge of designing phase locked loops, Delay locked loops.

UNIT-I

Introduction: Introduction to Phase locked loops (PLLs), Basic operation of PLL and DLL architectures. Steady state analysis of basic PLL architectures.

(05+05) Hrs

UNIT-II

Designing PFD and Charge pump: Phase detectors, Phase frequency detectors, Charge pump, Loop filters, Introduction to Charge pump based PLLs, Design methodology of charge pump based PLLs.

(05+05) Hrs

UNIT-III

Oscillators: Basic principles, Cross coupled oscillators, Voltage controlled oscillators, VCOs with wide tuning range, Basic concepts, of phase noise. Inverter based Ring oscillators, Basic differential ring oscillators.

(05+05) Hrs

UNIT-IV

Frequency synthesis: Introduction to frequency synthesis, Basic Integer N – Synthesizer, Divider design: Pulse swallow divider, Dual modulus divider,

Divider logic styles. Fractional N – Synthesizer: Basic concepts, Fractional divider using Delta sigma modulation technique. **(05+05) Hrs**

UNIT-V

Digital PLL (DPLL): Basic architecture of DPLL, Basic operation of Time to Digital conversion (TDC), Vernier TDC, Digitally controlled oscillator. Basics of Digital filters.

Clock and Data recovery circuits: Basic idea of clock and data recovery circuits, Bang-Bang Phase detector, Alexander phase detector, Hogge Phase detector.

(06+06) Hrs

Text Books:

1	Behzad Razavi	Design of CMOS Phase locked loops, from circuit level to Architecture level, Cambridge university press, 2020.
2	Behzad Razavi	RF microelectronics, 2nd Edition Pearson education 2012

Reference Books:

1	F. Gardner	Phaselock Techniques, John Wiley & Sons, 2005.
2	R. Best	Phase-Locked Loops : Design, Simulation, and Applications, McGraw Hill, 2003.

Course Outcomes: students will be able to

CO1: Analyze PLL architecture.

CO2: Design and Analyze PFDs and Charge pumps

CO3: Design and Analyze VCOs and Ring oscillators.

CO4: Design and Analyze dual modulus, integer -N and fractional dividers. and also design and analyze Charge pump based Integer N and fractional PLLs.

CO5: Understand the basics of Digital PLLs and Clock and data recovery circuits.

ACADEMIC YEAR: 2022-23

DSP Architecture

Contact Hours/ Week	: 2+0+2(L+P+T)	Credits :	3.0
Total Lecture Hours	: 26	CIE Marks :	50
Total Tutorial Hours	: 26	SEE Marks :	50
Course Code	: N2LVSE25		

Course Objective: To study DSP algorithms, architecture and interfacing of peripheral devices to the DSP processor.

UNIT- I

Introduction to Digital Signal Processing:

Introduction : Review of Digital Signal – Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation. Fixed point and Floating point processors.

Computational Accuracy in DSP Implementations: Number Formats for Signals and Coefficients in DSP Systems, Dynamic Range and Precision, Sources of Error in DSP Implementation.

(05+05) Hrs

UNIT- II

Architectures for Programmable Digital Signal – Processing Devices:

Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.

(05+05) Hrs

UNIT- III

Programmable Digital Signal Processors:

Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54XX, Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and Programming,

On – Chip Peripherals and Interrupts of TMS32OC54XX Processors,

Pipeline Operation in TMS32OC54xx Processor.

(05+05) Hrs

UNIT- IV

Implementation of Basic DSP Algorithms:

Introduction, The Q – notation, FIR Filters, IIR Filters, Interpolation and Decimation, Filters, PID controller,

Implementation of FFT Algorithms:

Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit – Reversed Index Generation & Implementation on the TMS32OC54xx.

(05+05) Hrs

UNIT- V

Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices:

Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O Direct Memory Access (DMA).

Interfacing and Applications of DSP Processors:

Introduction, Synchronous Serial Interface, A CODEC Interface Circuit, DSP Based Bio-telemetry Receiver, Speech Processing System, Image Processing System.

(06+06) Hrs

Text Book		
1	Avatar Singh and S. Srinivasan	Digital Signal Processing, Thomson Learning, 2004.
Reference Books:		
1	Ifeachor E. C., Jervis B.	Digital Signal Processing: A practical approach, W Pearson-Education, PHI, 2002.
2	B Venkataramani and M Bhaskar	Digital Signal Processors, TMH, 2nd, 2010.
3	Peter Pirsch	Architectures for Digital Signal Processing, John Weily, 2008.

Course Outcomes: The students will be able to

CO1: Apply the knowledge of DSP computational building blocks to develop DSP architecture or processor based applications.

CO2: Apply knowledge of various types of addressing modes, interrupts, peripherals and pipelining structure of TMS320C54xx processor.

CO3: Apply the knowledge of architecture and instruction set of DSP processor to write basic programs.

CO4: Develop algorithms to implement DSP algorithms on DSP processors.

CO5: Design Interfacing of Memory and I/O to DSP Processor.

Professional Elective-3

System on Chip Design

Contact Hours/ Week	:26+0+26(L+P+SDA)	Credits :	3.0
Total Lecture Hours	: 26	CIE Marks :	50
Total SDA Hours	: 26	SEE Marks :	50
Sub. Code	: N2LVSE31		

Course Objective (CO): This course will enable students to learn the System on Chip design with different approaches and understand the concepts of embedded memories and network on chip topologies.

UNIT- I

Motivation for SoC Design - Review of Moore's law, benefits of system-on-chip integration in terms of cost, power, and performance. Typical goals in SoC design – cost reduction, power reduction, design effort reduction, performance maximization. Productivity gap issues and the ways to improve the gap. Comparison on System-on-Board, System-on-Chip, and System-in-Package

System On Chip Design Process: Canonical SoC Design, System Design flow - waterfall design flow, Spiral design flow,Top-down vs Bottom up design flows and **Construct by Correction.**

(05+05) Hrs

UNIT- II

System level design issues

Specification requirement, Types of Specification. The Standard Model: - Soft IP vs Hard IP, The Role of Full-Custom Design in Reuse. Design for Timing Closure: Logic Design Issues. Design for Timing Closure: Physical Design Issues. Design for Verification: Verification Strategy. System Interconnect and On-Chip Buses. Design for Bring-Up and Debug. Design for Low Power. Design for Test: Manufacturing Test Strategies. Prerequisites for Reuse

(05+05) Hrs

UNIT- III

Macro Design Process: Overview of IP Design, Key Features, Planning and Specification, Macro design and Verification. Developing Hard Macros: Overview, Design Issues for Hard Macros, The Hard Macro Design Process, Productization of Hard Macros.

(05+05) Hrs

UNIT- IV

SoC Verification: -Verification technology options, Verification methodology, Verification languages, Verification IP Reuse, approaches. Verification and Device Test, Verification Plans. UVM oveview VLSI Packaging: Introduction, Packaging, Power Distribution, Input/Output, Chip-Package Co-design.

(05+05) Hrs

UNIT- V

Embedded Memories –cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence. MESI protocol and Directory-based coherence.

Interconnect architectures for SoC: Bus architecture and its limitations. Network on Chip (NoC) topologies.Mesh-based NoC. Routing in anNoC. Packet switching and wormhole routing.

MPSoCs: Introduction to MPSoCs, Techniques for designing MPSoCs.

(06+06) Hrs

Text Books:

1	Sudeep Pasricha and NikilDutt	On-Chip Communication Architectures: System on Chip Interconnect , Morgan Kaufmann Publishers, 2008
2	Rao R. Tummala, MadhavanSwaminathan	Introduction to system on package sop-Miniaturization of the Entire Syste, McGraw-Hill, 1st Edition, 2008.
3	James K. Peckol	Embedded Systems: A Contemporary Design Tool , Wiley, 1st Edition, 2007.
4	Michael Keating, Pierre Bricaud	Reuse Methodology Manual for System on Chip design s , Kluwer Accademic Publishers, 2nd edition, 2008
5	Sung-Mo Kang, Yusuf Leblebici	CMOS Digital Integrated Circuits , Tata Mcgraw-Hill, 3rd Edition, 2004.

Course Outcomes: Students will be able to

CO1: Describe the benefits and different design process of SoC.

CO2: Understand System-Level Design Issues, Rules and Tools

CO3: Identify and select an appropriate macro design style for SOC design

CO4: Analyze the various methods of SOC verification issues and packaging techniques.

CO5: Analyze cache protocols, NOC topology and describe the design concepts of different types of MPSoCs.

CO6: Carry on design of selected circuit for a particular application using appropriate tool. Prepare the report.

System Verilog

Contact Hours/ Week	: 2+0+2(L+P+SDA)	Credits :	3.0
Total Lecture Hours	: 26	CIE Marks :	50
Total SDA Hours	: 26	SEE Marks :	50
Course Code	: N2LVSE32		

Course Objectives: To impart the knowledge on system Verilog language to design, assertion and verify functionality of the system.

UNIT- I

Basics of Verification: Difference between ASIC verification and ASIC testing, Verification basics, Test benches, Layered Organization of Test benches. Importance of hardware verification languages and methodologies. **System Verilog data types and typedefs:** System Verilog data types, enhanced literal numbers syntax, 4-state and 2-state types, typedefs, enum, struct data type, Type parameters, $unit and $root. Packages, strings, static and dynamic type casting, Random number generation. **(05+05)Hrs**

UNIT- II

System Verilog operators, loops, jumps, functions: loops and jumps in system verilog, introduction to different always blocks, system verilog enhancements to tasks and functions, system verilog priority and unique modifiers for case and if statements, ‘time scale, system verilog time unit and time precision.

Structs, Unions, Packed and Unpacked Arrays, Semaphores and Mailboxes: Structs and its assignments, packed and unpacked arrays, array indexing, structs and packed structs, Unions and packed unions, dynamic arrays and methods, for each loop, associative arrays and methods, queues and concatenation operations, queue methods, semaphores and methods, Mail boxes and methods, bounded and unbounded mail boxes. **(05+05)Hrs**

UNIT- III

Class and Randomization: System verilog class basics, class declaration, class members and methods, class handles, class object construction, super and this keywords, object handles, user defined constructors, class extension and inheritance, chaining new() constructors, overriding class methods, extending class methods, local and protected keywords, constrained random variables, directed vs random testing, rand and randc class data types, randomize-randomizing class variables, random case, built-in-randomization methods, random sequence and examples.

(05+05)Hrs

UNIT- IV

Interfaces: Interface overview, generic interfaces, interfaces vs records, how interfaces work, requirements of good interface, interface constructs, interface mode ports.

Program block: Fundamental test bench construction, program blocks, program block interaction with modules, final blocks, Test-bench stimulus/Verification vector timing strategies.

Clocking: Clocking blocks, clocking skews, clocking block scheduling, fork-join processes.

(05+05)Hrs

UNIT- V

Constrained Random variables, Coverage, Methods and interfaces: Randomization constraints, simple and multi-statement constraints, constraint distribution and set membership, constraint distribution operators, external constraints, covergroups, coverpoints, coverpoint bins and labels, cross coverage, covergroup options, coverage capabilities. Virtual class, why to use virtual class, virtual class methods and restrictions, polymorphism using virtual methods, pure virtual methods, pureconstraints, passing type parameters, virtual interfaces.

(06+06)Hrs

Text Books:

1	Christian B Spear	"SystemVerilog for Verification: A guide to learning the Testbench language features", Springer publications, 3 rd edition.
2	VijayaRaghavan	"SystemVerilog Assertions", Springer publications, 2005
3	Sutherland	"Systemverilog for Design", Springer publications

Course Outcomes: Students will be able to

CO1: Identify and use appropriate data types for system Verilog programming.

CO2: Select and apply appropriate program constructs for System design.

CO3: Select and apply appropriate methods to write test benches.

CO4: Identify, select and apply different clocking schemes for optimization of designs.

CO5: Explain Constrained Random variables, Coverage, Methods and interfaces

CO6: Carry on design of selected circuit for a particular application using appropriate tool. Prepare the report.

Low Power VLSI Design

Contact Hours/ Week	: 2+0+2(L+P+T)	Credits:	3.0
Total Lecture Hours	: 26	CIE Marks:	50
Total Tutorial Hours	: 26	SEE Marks:	50
Course Code	: N2LVSE33		

Course Objective: To analyze and estimate power at different abstraction levels of CMOS VLSI.

UNIT- I

Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices. **Device & Technology Impact on Low Power:** Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

(05+05) Hrs

UNIT- II

Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.

(05+05) Hrs

UNIT- III

Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

Low Power Design Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library.

(05+05) Hrs

UNIT- IV

Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. **Low power Architecture & Systems:** Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

(05+05) Hrs

UNIT- V

Low power Clock Distribution, **Algorithm & Architectural Level Methodologies:** Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

(06+06) Hrs

Text Books:

1	Kaushik Roy, Sharat Prasad	"Low-Power CMOS VLSI Circuit Design" Wiley, 2000
2	Gary K. Yeap	"Practical Low Power Digital VLSI Design", KAP, 2002.
3	Rabaey, Pedram	"Low Power Design Methodologies" Kluwer Academic, 1997.

Course Outcomes: Students will be able to

CO1: Analyze the impact of low power in VLSI circuits

CO2: Recognize Role of simulation possible at various levels of design

CO3: Explain Relationship of probability while calculating power dissipation of circuits

CO4: Apply Power reduction techniques at circuit and architectural level.

CO5: Discuss different clock distribution techniques in low power VLSI design.

Wireless Sensor Network

Contact Hours/ Week	: 2+0+2(L+P+SDA)	Credits :	3.0
Total Lecture Hours	: 26	CIE Marks :	50
Total SDA Hours	: 26	SEE Marks :	50
Course Code	: N2LVSE34		

Course Objectives: This course will enable students to learn about WSN technology that emphasis on standardization of basic sensor systems, medium access protocols and address network layer issues.

UNIT- I

Introduction and overview of Wireless Sensor Network(WSN), commercial and scientific applications of WSN, Category of Applications of WSN, Challenges for WSN, Enabling Technologies for WSN.

(05+05) Hrs

UNIT- II

Single node Architecture: Hardware Components, Energy consumptions of Sensor nodes, Operating Systems and Execution Environments, Examples of Sensor nodes, Network Architecture : WSN Scenarios, Optimization Goals and figure of Merits, Design principles for WSNs, Service Interface for WSNs, Gateway Concepts.

(05+05) Hrs

UNIT- III

Physical Layer: Wireless Channel and Communication Fundamentals, Physical Layer & Transceiver Design Considerations in WSN, MAC Protocols: Fundamentals, MAC Protocol for WSNs, IEEE802.15.4 MAC Protocol, and Routing Protocols: Gossip and agent based unicast protocols, Energy Efficient Unicast, Broadcast and Multicast, Geographic Routing, Transport Control Protocols: Traditional Protocol, Design issues.

(05+05) Hrs

UNIT- IV

Sensor tasking and Control: Introduction –Based Sensor Tasking, Joint Routing Information Aggregation, Sensor Network databases: Challenges Query Interfaces, In-Network Aggregation, Data Centre Storage.

(05+05) Hrs

UNIT- V

Operating System for Sensor Networks: Introduction, Design Issues, Examples of Operating Systems, Node Level Simulators, Performance and Traffic Management Issues: WSN Design Issues, Performance modelling of WSNs, Emerging Applications.

(06+06) Hrs

Text Books:

1.	Kazem Sohraby,Daniel Minoli,Taieb Znati	“Wireless Sensor Networks: Technology, Protocol and Applications” John wiley & sons.
2.	Holger Karl, Andreas Wiling	“Protocols and architectures for wireless sensor networks” John wiley & sons

Reference Books:

1.	Feng Zaho, Leonidas Guibas	,”Wireless sensor Networks; An Information Processing Approach”,Elsevier
2.	C.S. Raghavendra, Krishna, M,Shivalingam, Taieb Znati	“Wireless sensor networks”, Springer Verlag.
3.	H.Edgar,Jr.Callaway	“Wireless sensor networks, architecture and Protocols “, CRC Press.

Course Outcomes: Student will be able to

CO1: Familiarize about WSN, architecture, and technologies.

CO2: Explain Wireless sensor platforms: Hardware and Software

CO3: Understand Communication architecture and protocols for WSN (MAC, Link, Routing)

CO4: Explain Energy management

CO5: Understand sensor data acquisition, processing and handling.

CO6: Design the circuit for a particular application using appropriate tool. Prepare the report.

Interference and noise control techniques in ESD

Contact Hours/ Week	: 2+0+2(L+P+T)	Credits :	3.0
Total Lecture Hours	: 26	CIE Marks :	50
Total Tutorial Hours	: 26	SEE Marks :	50
Course Code	: N2LVSE35		

Course Objectives: This course aims at understanding the fundamentals of Interference and Noise Control Techniques in Electronic Design.

UNIT- I

Basic Concept of Instrumentation Design: Needs Analysis :with respect to systems deployed in; Medical, Industrial, Test and Measurement, Home Appliances, Military Functional requirements & Specifications, Impact on the design due to adverse Electrical, Thermal and Mechanical Operational Environments.

Noise Sources: Electrical, Magnetic, RF, Static, Ground Loops, Shielding, near and far field, shielding effectiveness, absorption and reflection loss, shielding with magnetic material, contact protection, glow and arc discharges, loads with high inrush current, Inductive and resistive load contact protection networks for inductive loads, intrinsic noise sources

Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD.

(05+05) Hrs

UNIT- II

EMI / EMC STANDARDS: ESD, inductive charging human body model, ESD protection in equipment design, Preventing ESD entry, Transient Hardened software Design, Hardening Sensitive Circuits, input filters, clamping suppressors

Civilian standards: FCC, CISPR, IEC, EN, Military standards - MIL STD 461D/462, EMI Test Instrument /Systems, EMI Shielded Chamber, Open Area Test Site, TEM Cell, Sensors/Injectors/Couplers, Test beds for ESD and EFT. **(05+05) Hrs**

UNIT- III

Electronic design guidelines: Noise in electronic circuits**.** Capacitive and inductive coupling and effect of shield, shielding to prevent magnetic radiation, co-axial and twisted pair cable, grounding, safety ground, signal ground, single and multi point ground, Hybrid ground, grounding of cables shields, Ground loops and low frequency and high frequency analysis of common mode signals, guard shields Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting. **(05+05) Hrs**

UNIT- IV

PCB Design Guidelines. NEMA, DIN, BSI, ANSI standards Index protection (IP), cable design guidelines; Printed circuit board design guideline, layout scheme, grid systems, PCB size, Design rules for digital circuits, and Design rules for analog circuits, single and multilayer PCB, CE / Underwrites Laboratories (UL) Compliance.

PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models.

(05+05) Hrs

UNIT- V

Failure Mechanism and Faulty Tolerance Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

Test for Reliability: Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

(06+06) Hrs

Text Book:

1	Henry OTT	Noise reduction Techniques in Electronics Circuit, Wiley International, Second ed., 2009.

Reference Books:

1	W. Prasad Kodali	Engineering Electromagnetic Compatibility: Principles, Measurements and Technologies and Computer Models, Wiley, IEEE Press, 2nd Edition, 2001.
2	Henry W. Ott	Electromagnetic Compatibility Engineering, John Wiley and Sons, 1st Edition, 2009.
3	Clayton. R. Paul	Introduction to Electromagnetic Compatibility, John Wiley and Sons, 2nd Edition, 2006.
4	Bernhard Keiser	Principles of Electromagnetic Compatibility, Artech house, 3rd Edition, 1998.
5	Balguruswamy	Reliability Engineering, TATA McGraw-hill Publication, 3rd Edition, 2005
6	Walter C. Bosshart	Printed Circuit Board, Tata McGraw-Hill publication, 3rd Edition, 2009.
7	Patrick D.T. O'Connor, David Newton and Richard Bromley	Practical Reliability Engineering, John Wiley & Sons, 4th Edition, 2002

Course Outcomes: The students will be able to

CO1: Analyze the requirement of Instrument and systems. Identify the sources of Noise
CO2: Discuss the various EMI / EMC STANDARDS
CO3: Design various electronic circuits , noises identification and appropriate elimination methods related to instrument and system
CO4: Discuss the various Guidelines for PCB Design
CO5: Estimate, analyze, improve the reliability of instrument and system

Open Elective 1

Embedded Systems

Contact Hours/ Week	: 3+0+0 (L+P+T)	Credits :	3.0
Total Lecture Hours	: 40	CIE Marks :	50
Total Tutorial Hours	: 0	SEE Marks :	50
Course Code	: N2OE01		

Course Objective: To impart the knowledge of Cortex M3 and M4 based Microcontroller Architecture, Exception and Interrupt behavior, Programming and configuring on chip peripherals and interfacing of I/O devices.

UNIT- I

Introduction: Basic architecture of Embedded Systems, Microprocessors and Microcontrollers, Von-Neumann and Harvard Architectures, History of ARM family of processors, Architecture and Features of ARM Cortex M3 and M4 processors. Programmer's model: Operation Modes and States, General purpose Registers, Special function Registers, Behavior of APSR. Pipelining, Prefetch unit and Branch target forwarding in ARM cortex M3 and M4 processors. Memory system: Memory map.

(05+05) Hrs

UNIT- II

Memory Format: Memory endianness, data alignment and unaligned data access support, Bit-band operation in ARM Cortex M3 and M4 processors. Embedded Software development-1: Embedded Software Development and compilation flow. Data types in C – programming used for Cortex M4 processors. Introduction to Cortex M3 based Microcontroller: Features, Memory map, basic configuration and programming of GPIO. Interfacing Input output devices to Cortex M3 based Microcontroller-1: LEDs and Switches, C-Programming examples.

(05+05) Hrs

UNIT- III

Instruction set: Operation and addressing modes of MOV instruction, Arithmetic instructions, Logical instructions, Memory access instructions, Program flow control instructions, Shift and rotate instructions, Data conversion instructions, Bit-field processing instructions, compare and test instructions. Use of suffix in instructions. ARM Assembler directives, Assembly level programming examples. Interfacing Input output devices to Cortex M3 based Microcontroller-2: 7-segment Display, Push button keys, mxn matrix keypad. Programming examples (Both assembly and C).

(05+05) Hrs

UNIT- IV

Embedded Software development-2: Program flow (Software Flow).
Exceptions and Interrupts: Overview of Exceptions and Interrupts, Exception types, Vector table and Reset status, Exception entrance sequence, Exception handler execution, Exception return, Interrupt latency, NVIC registers for interrupt control, Exception handlers in C and assembly level programming, Stack Frames, Exceptions entrance and stacking, Exception return and unstacking. Programming Examples (Both assembly and C). System control blocks of Cortex M3 and M4 based Microcontroller: Reset, Brown-out detection and External interrupt inputs.
Peripherals in Cortex M3 and M4 based Microcontroller: Configuration and programming (both assembly and C) Nested Vectored Interrupt Controller (NVIC) and Timers.

(05+05) Hrs

UNIT-V

Configuration and programming (Only C) PWM unit, Watchdog timer, Analog to Digital Converter (ADC), Digital to Analog Converter (DAC), Universal Asynchronous Receiver Transmitter (UART) , SPI and I2C. Case study: Temperature control system, Traffic control systems, Washing machine control system.

(06+06) Hrs

Text Books:

1	Joseph Yiu	The Definitive guide to ARM Cortex M3 and Cortex M4 processor, Elsevier, 3rd Edition, 2013.
2	Cortex-M Technical Reference Manual. revision r1p1	
3	LPC17xx Reference Manual.	

Reference Book:

1	Ming-Bo Lin	An Introduction to Cortex-M3-Based Embedded Systems: Cortex-M3 Assembly Language Programming, Createspace Independent Publishing Platform, 2019.

Course Outcomes: Students will be able to

CO1: Explain the architecture of ARM cortex M3 and M4 Architecture and differentiate Microcontrollers and Microprocessors.
CO2: Explain the Memory system of ARM Cortex M3 and M4 based Processors and Develop the program for ARM cortex M3 and M4 based microcontrollers in order to Interface Input and output devices such as LED and Switches.
CO3: Explain the operation of the Instruction set of the ARM cortex M3 and M4 based processors and Develop the program for ARM cortex M3 and M4 based microcontrollers in order to Interface Input and output devices such as 7-segment Display, Push button keys, mxn matrix keypad.
CO4: Explain the concept of Exceptions and interrupts and Develop the program to configure peripherals of ARM cortex M3 and M4 based microcontrollers such as External interrupts, NVIC and Timers,
CO5: Develop the program to configure peripherals of ARM cortex M3 and M4 based microcontroller and to develop the program for ARM cortex M3 and M4 based microcontrollers in order to Interface Input and output devices.

CMOS RF Circuit Design

Contact Hours/ Week	: 3+0+0(L+P+T)	Credits :	3.0
Total Lecture Hours	: 40	CIE Marks :	50
Total Tutorial Hours	: 0	SEE Marks :	50
Course Code	: N2OE02		

Course Objective: To impart the knowledge on designing CMOS RF Circuit.

UNIT- I

Introduction to RF Design and Wireless Technology: Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Inter-symbol interference, random processes and noise, Sensitivity and dynamic range, conversion of gains and distortion, characteristics of passive IC components, resistor, capacitor and inductor.

(05+05) Hrs

UNIT- II

Transceiver Architectures: Receiver Architecture: Heterodyne, Homo dyne, Image Reject Receiver and Transmitter Architecture. Transmitter Architecture: Direct Conversion Transmitters, Two-step transmitters.

Single stage amplifiers: Common source stage – with resistive load, Diode connected load, current source load, Triode load, Source degeneration. Source follower, Common gate stage, Cascode stage.

(05+05) Hrs

UNIT- III

Differential amplifiers: Single ended differential operation, Basic differential pair, common mode response, Differential pair with MOS loads, Current mirrors: Basic current mirrors, Cascode current mirrors, Active current mirrors.

Low noise Amplifier design: CS stage: Inductive load, Resistive Feedback, Inductive degeneration. Variants of CS LNA, Noise – Cancelling LNAs, Differential LNAs. Non linearity Calculations in LNAs.

(05+05) Hrs

UNIT- IV

Mixers: Mixer Nose Figures, Port – Port Feed through, Single –balanced and double balanced Mixers, Introduction to Passive and Active Mixers.

Oscillators: General Principles: Feedback view, One-Port view, Cross-Coupled Oscillator, Three – Point Oscillators. Voltage Controller Oscillators (VCO): Tuning Limitations, Effect of varactor Q, VCOs with wide tuning Range. Effect of Phase Noise, Low noise VCOs.

(05+05) Hrs

UNIT- V

Phase Locked Loop (PLL): Type – I PLLs: VCO phase Alignment, Dynamics of Type – 1 PLLs, Frequency Multiplication, Draw backs of Type – 1 PLL. Type-II PLLs: Phase/Frequency Detectors, Charge Pumps, Charge-Pump PLLs, Transient Response.

Integer N Frequency Synthesizer: Basic integer N Frequency Synthesizer, Setting behavior, Spur reduction technique.

Distributed Systems: Transmission lines, reflection coefficient, the wave equation, examples, Lossy transmission lines, Smith charts – plotting gamma.

(06+06) Hrs

Text Books:

1	B. Razavi	RF Microelectronics, PHI, 2nd Edition, 2011
2	R. Jacob Baker, H.W. Li, D.E. Boyce	CMOS Circuit Design, layout and Simulation, PHI, 1998.
3	Thomas H. Lee	Design of CMOS RF Integrated Circuits Cambridge University press, 2nd Edition, 2003.
4	Y.P. Tsividis	Mixed Analog and Digital Devices and Technology, TMH, 1996.

Course Outcomes: Students will be able to,

CO1: Explain performance parameters to be considered for the design of RF circuits.

CO2: Design single stage amplifiers. Discuss various Transceiver architecture and bandwidth estimation techniques.

CO3: Analyse and Design differential amplifier and of low noise amplifiers

CO4: Identify and explain the general considerations of mixers and Oscillators.

CO5: Discuss the modelling of various devices at RF Frequency and general principles of oscillators and PLL. Design PLL models using Matlab Prepare the report.